Driving Wide-Bandgap Transistors To The Limits!

MINDCET.
Custom
Integrated Power
Management
Solutions

PwrSOC 2018, Taiwan

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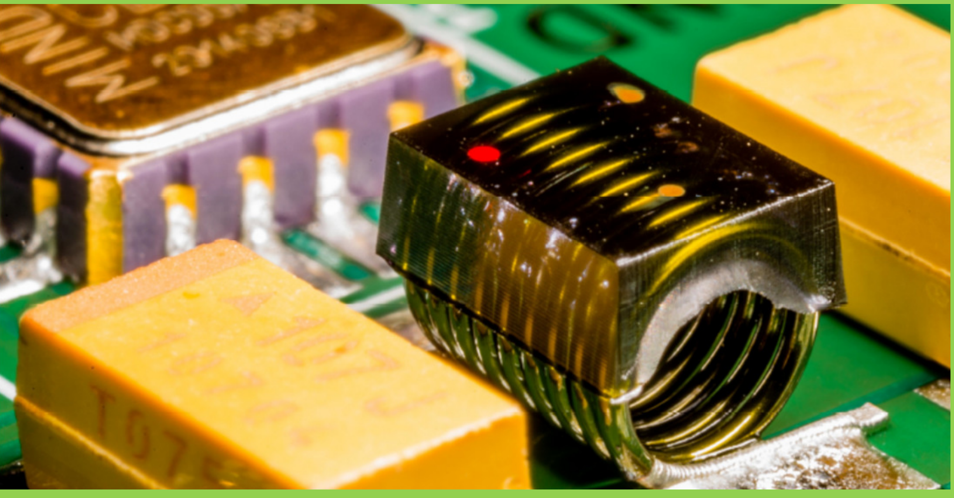
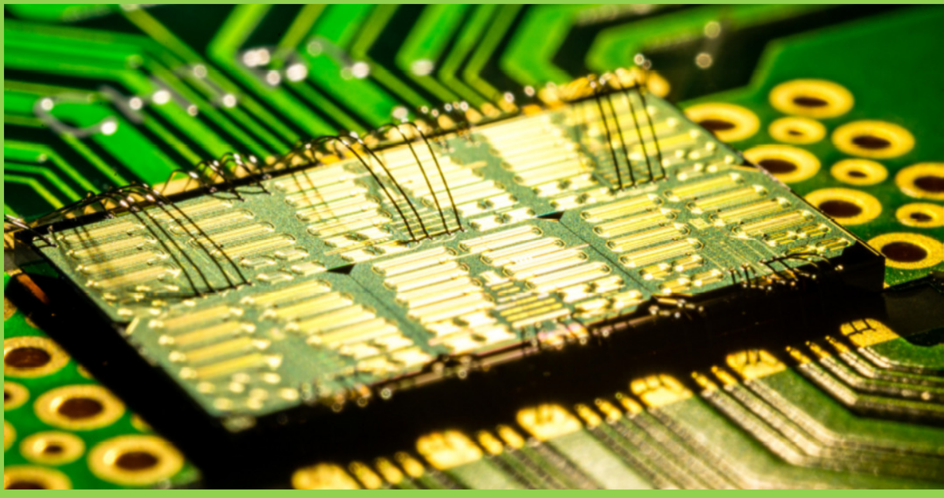




Wide bandgap is trending

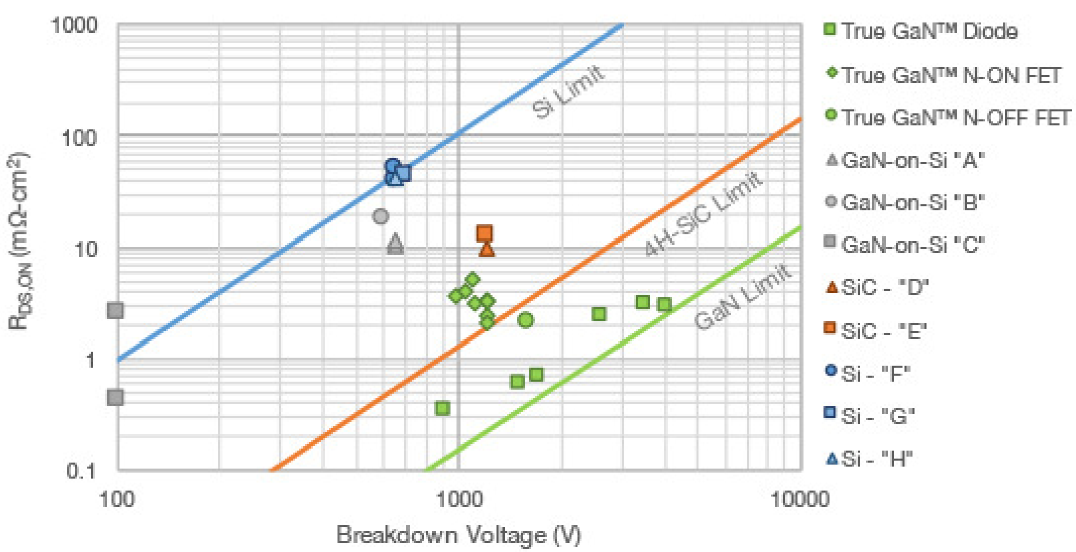
APEC 2018 proceedings => 710 papers & presentations

- #SiC => 474 hits (67%)
- #GaN => 356 hits (50%)
- #IGBT => 167 hits (23%)
- #CMOS =>48 hits in (7%)
- #superjunction =>14 hits (2%)
- #DMOS => 12 hits (1.6%)

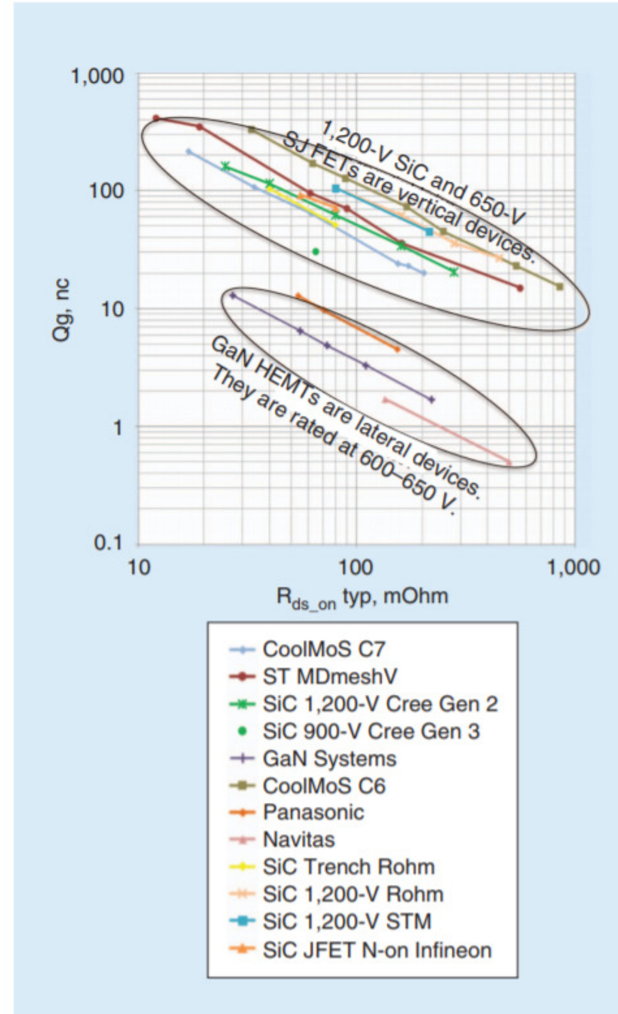
Is wide bandgap better?

Comparison

- In theory: yes :
  - smaller specific Rdson for GaN and SiC
  - Lower gate charge * Rdson
- In practice: depends.



Source : nexgen powersystems



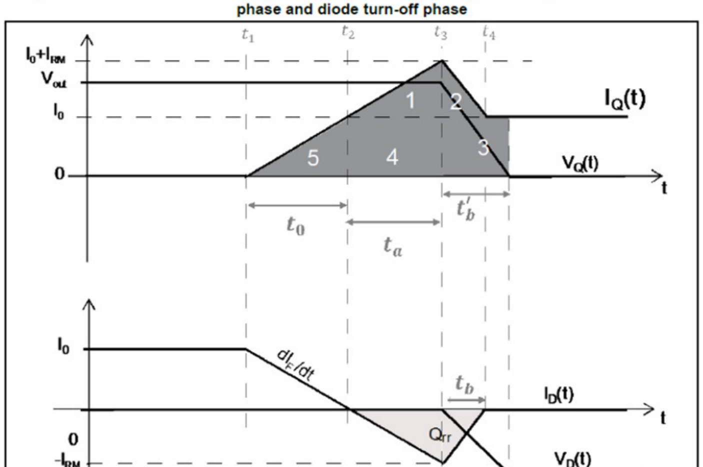
Source : IEEE Power Electronics, Vol 5, No 2, june 2018

Power loss revisited

Power losses revisited

- Gate loss : $P_g = Q_g * V_g * f_{sw}$
- C_{oss} loss : $Pc_{oss} = C_{oss} * V_{sw}^2 * f_{sw}$
- R_{dson} loss : $P_{rds} = R_{dson} * I_{out}^2$
- Switching loss : $P_{sw} = V_{sw} * I_{out} * (t_r+t_f) * f_{sw}/2$
- (Reverse recovery loss : $P_{rr} = (I_{out}*t_a+Q_{rr})* V_{sw} * f_{sw}$)

Figure 13: Ideal current and voltage waveforms of a switching cell during MOSFET turn-on phase and diode turn-off phase



Source : AN5028 ST

Benchmarking of GaN vs SiC vs Si

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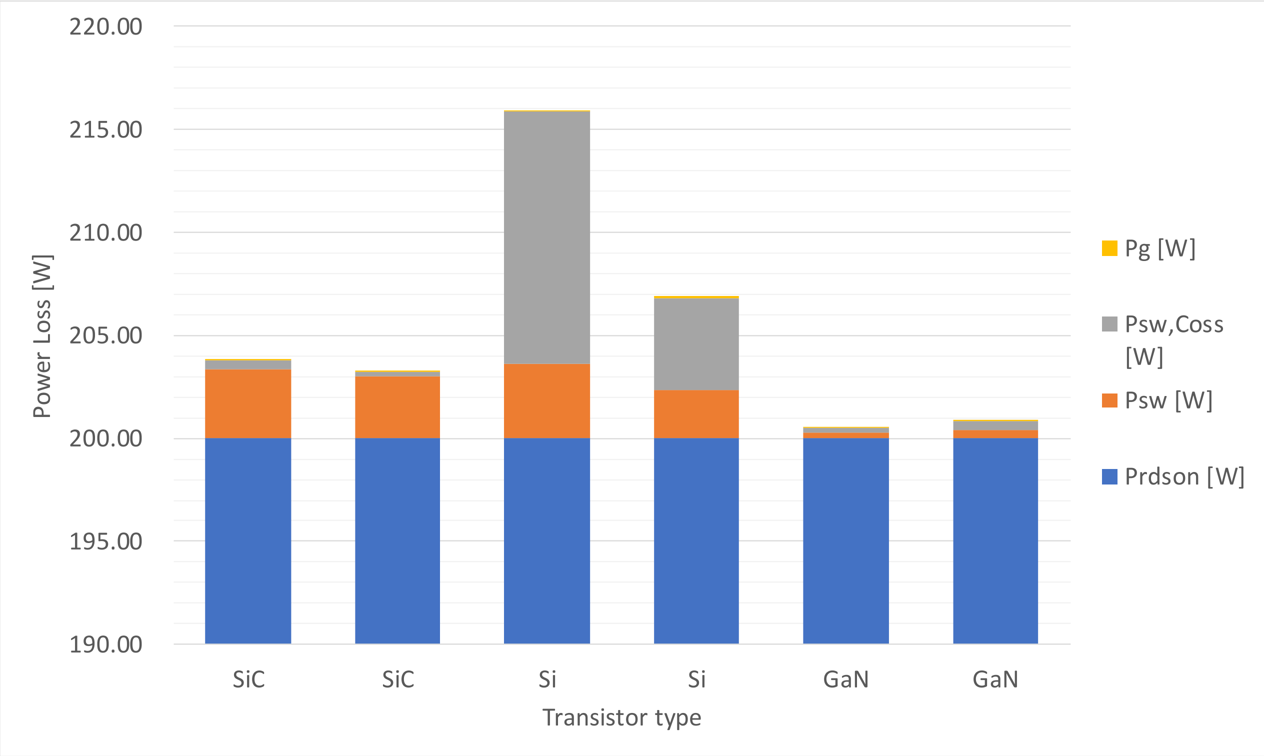
Manufacturer	Type	Type no.	Configuration	Vmax [V]	Imax [A]	Rgint [Ohm]	dVgs [V]	Qg [uC]	Rdson [mOhm]	Rdson * Qg [mOhm.uC]	Coss [nF]	Coss/Qg [nF/uC]	Tr [ns]	Tf [ns]
Cree	SiC	CAS300M12BM2	Halfbridge	1200	404	3	25	1	5	5.00	2.55	2.55	68	43
Semikron	SiC	SKM350MB120SCH15	Halfbridge	1200	523	0.6	18	1.5	5.6	8.40	1.10	0.73	50	50
IXYS	Si	IXFN32N120P	single fet	1200	32	0.83	10	0.36	310	111.60	1.10	3.06	62	58
Microsemi	Si	APT28M120B2	single fet	1200	29		10	0.3	450	135.00	0.28	0.92	31	48
GaN Systems	GaN	GS66508B	single fet	650	30	1.13	5	0.0058	50	0.29	0.14	24.48	3.7	5.2
Visic	GaN	VMHB120D	halfbridge	1200	180		12	0.0096	40	0.38	0.28	29.17	4	10

Benchmarking of GaN vs SiC vs Si

1kHz / 600V / 100A, all Rdson normalized to 20 mOhm

Manufacturer	Type	Type no.	Sum [W]
Cree	SiC	CAS300M12BM2	203.80
Semikron	SiC	SKM350MB120SCH15	203.23
IXYS	Si	IXFN32N120P	215.93
Microsemi	Si	APT28M120B2	206.89
GaN Systems	GaN	GS66508B	200.52
Visic	GaN	VMHB120D	200.82



Benchmarking of GaN vs SiC vs Si

10kHz / 600V / 100A, all Rdson normalized to 20 mOhm

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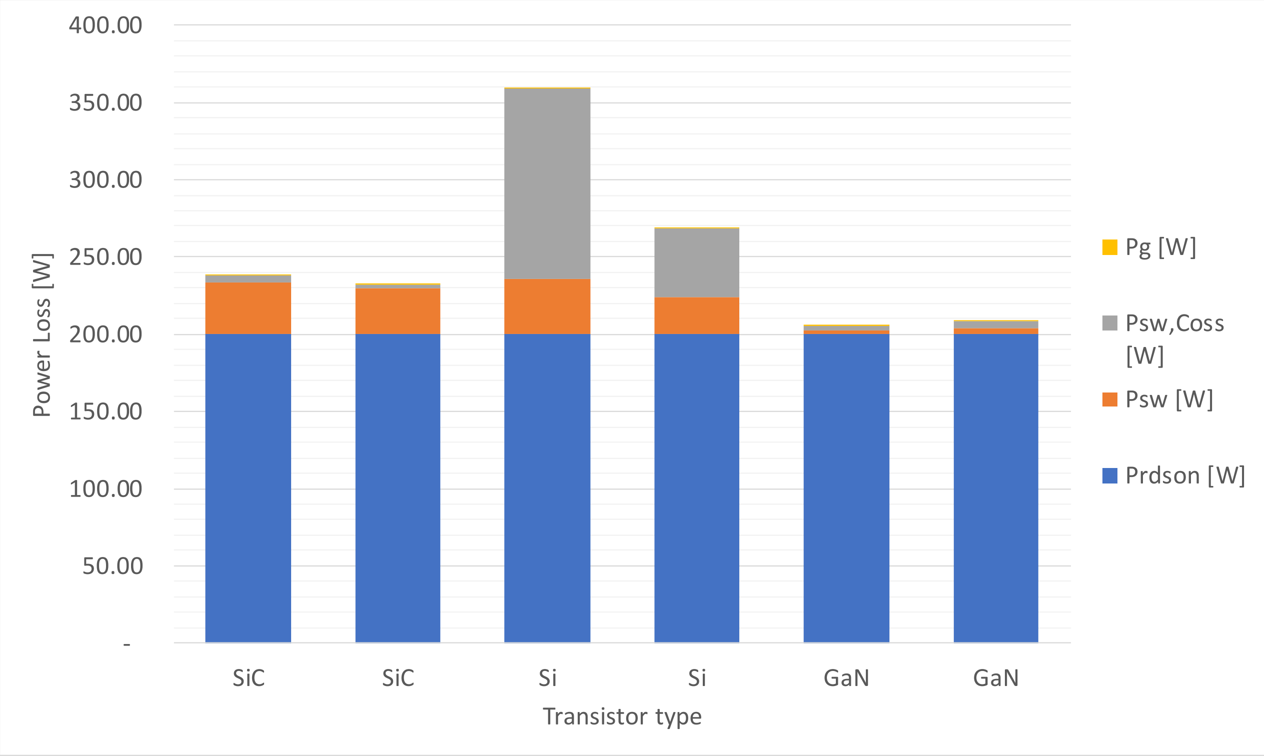
Manufacturer	Type	Type no.	Sum [W]
Cree	SiC	CAS300M12BM2	237.95
Semikron	SiC	SKM350MB120SCH15	232.29
IXYS	Si	IXFN32N120P	359.32
Microsemi	Si	APT28M120B2	268.93
GaN Systems	GaN	GS66508B	205.23
Visic	GaN	VMHB120D	208.23



Benchmarking of GaN vs SiC vs Si

100kHz / 600V / 100A, all Rdson normalized to 20 mOhm

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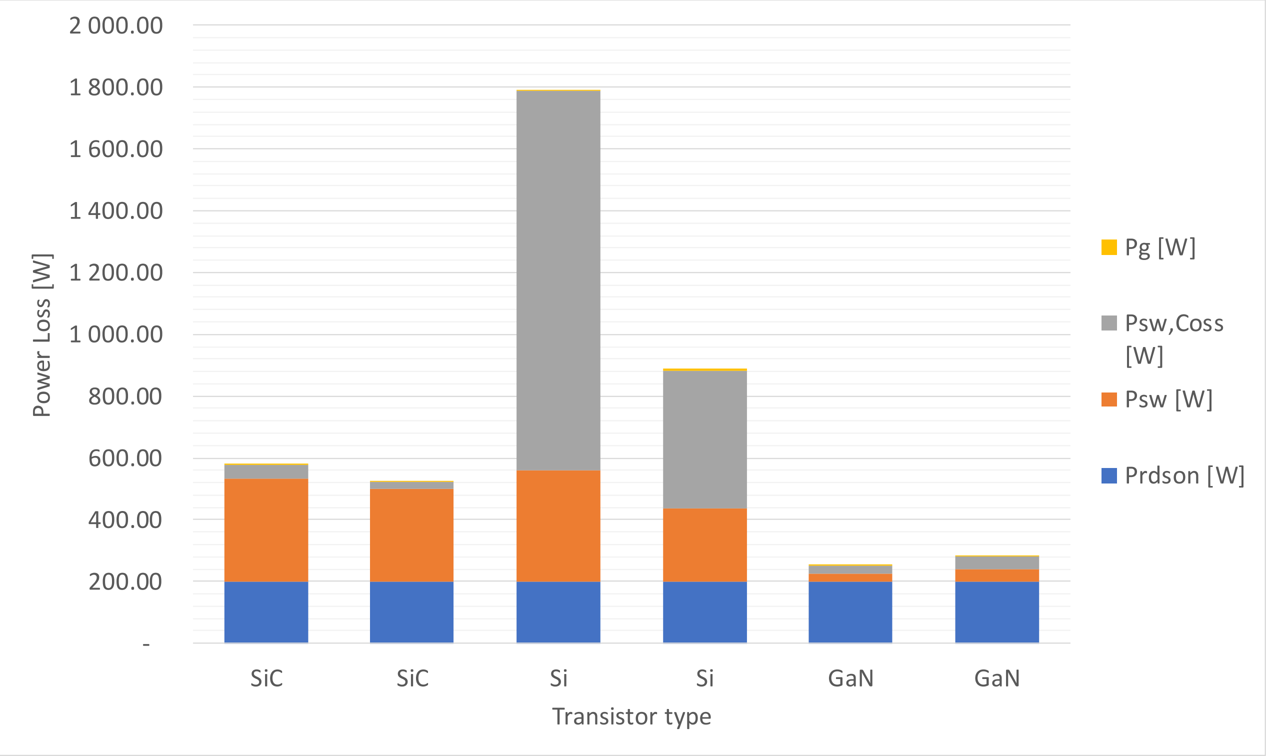
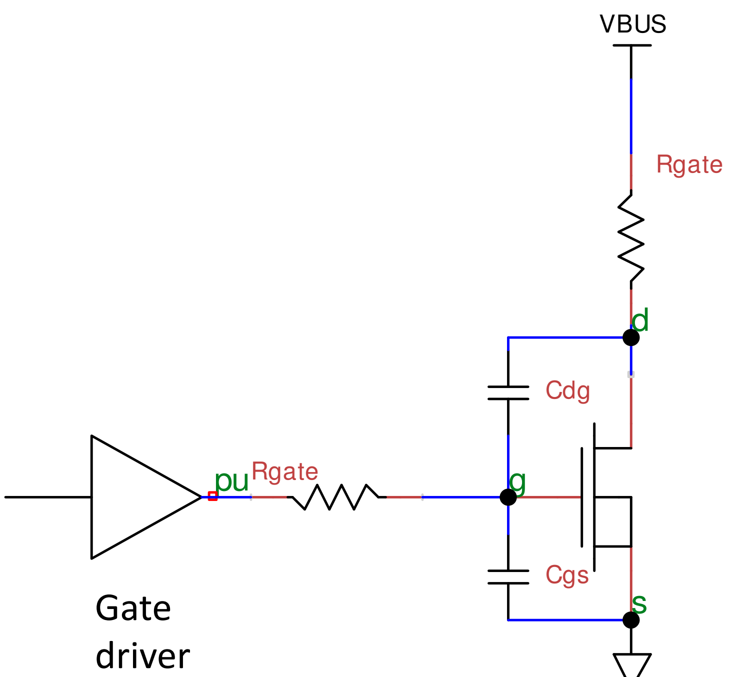
Manufacturer	Type	Type no.	Sum [W]
Cree	SiC	CAS300M12BM2	579.53
Semikron	SiC	SKM350MB120SCH15	522.93
IXYS	Si	IXFN32N120P	1 793.18
Microsemi	Si	APT28M120B2	889.25
GaN Systems	GaN	GS66508B	252.27
Visic	GaN	VMHB120D	282.34

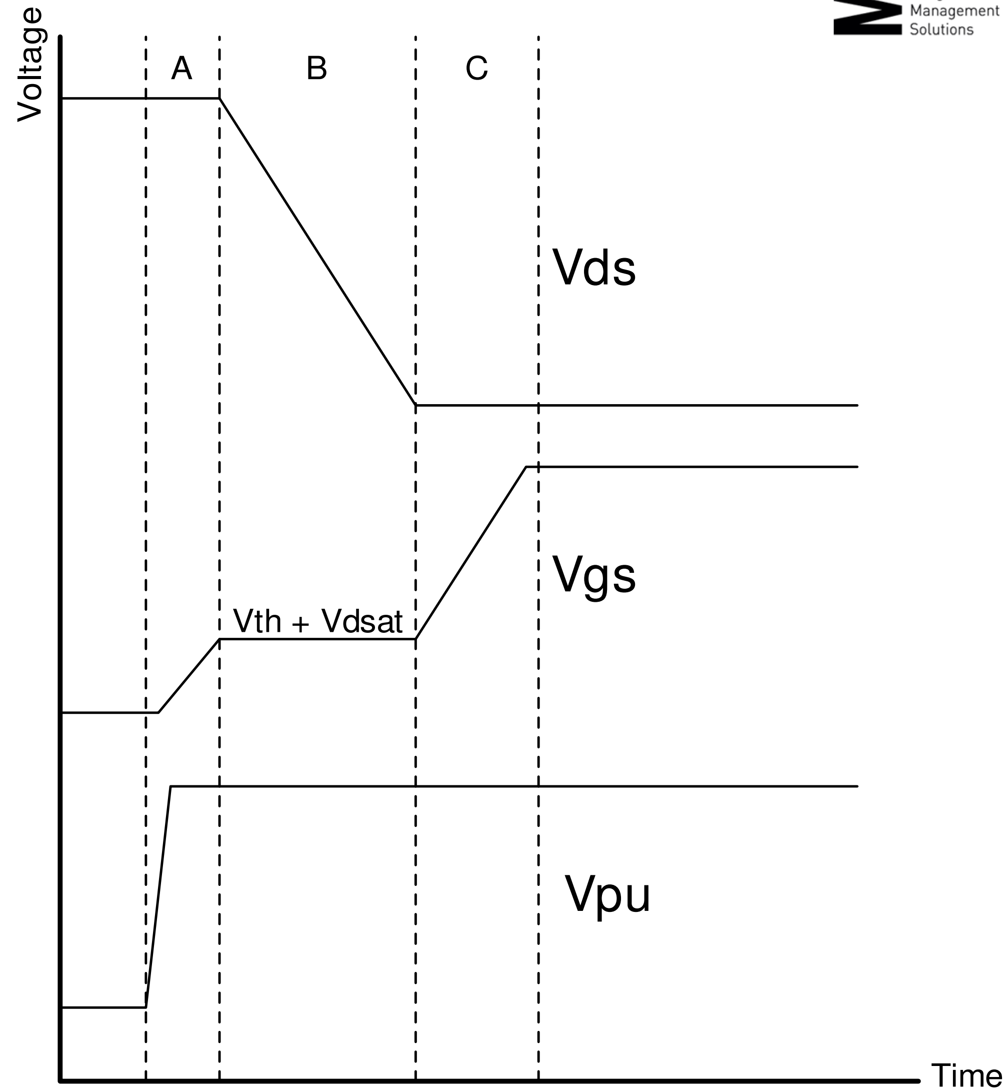


Conclusions

- Regarding driver power loss, <10kHz, there seems little value for going to SiC or GaN vs Si
- Above 10kHz, SiC or GaN perform similarly
- Where is the benefit ?
  - **Package power density @ 1200V**
    - SiC (SKM350MB120SCH15) : 19.5 Ohm*mm² (1200V)
    - GaN (VM40HB120D) : 125 Ohm * mm² (1200V)
    - GaN (GS66508B) : 3 Ohm*mm² (650V)
    - Si (APT28M120B2) : 244 Ohm*mm² (1200V)
  - No (or little) **reverse recovery**
    - yielding lower switching losses
    - Lower current spikes during switching transitions => potentially better EMI
  - **Higher temperature capability** for GaN and SiC

Gate switching revisited





Gate switching

- A : precharge from 0 (or negative voltage) to Vth + Vdsat
  - Ideally as short as possible
- B : defines slope of Vds. In case of inductive loads pulling Vds in the right direction, miller plateau is not present (and helps the efficiency!)
- C : charge from Vth+Vdsat to full Vgs.
  - Ideally as short as possible : it is interesting to reach the steady state Rdson as fast as possible (Rdson losses)

Why Rgate ?

- Gate loss : $P_g = Q_g * V_g * f_{sw}$
  - Dissipating in the gatedriver is costly (die area) or impossible (eg lack of cooling)
  - Putting Rg keeps power outside the driver
- Gate source parasitic inductance
  - $e = L_{gs}\, di_{gate}/dt$
  - Either limit inductance (impossible for OTS power FETs)
  - Or dI/dt, by adding Rg
- Lack of kelvin gate connections
  - $e = L_s\, di_{source}/dt$
  - Slow down switching Vds at cost of power, but slower Ids change as well.

Benchmarking of GaN vs SiC vs Si

100kHz / 600V / 100A, all Rdson normalized to 20 mOhm

Manufacturer	Type	Type no.	Pg [W]
Cree	SiC	CAS300M12BM2	0.63
Semikron	SiC	SKM350MB120SCH15	0.76
IXYS	Si	IXFN32N120P	5.58
Microsemi	Si	APT28M120B2	6.75
GaN Systems	GaN	GS66508B	0.01
Visic	GaN	VMHB120D	0.02

- In general the power devices are cooled well (liquid cooling), in contrast to the gate driver board
  - May be enclosed
  - May not have active cooling
- Pgate becomes problematic at high frequency
  - Putting Rgate keeps power external to the gate driver
  - Practical board limit 2..3 W

Benchmarking of GaN vs SiC vs Si

Why Rgate ?

- For high frequency (>10kHz) driving a HV Si MOS without Rgate is too (real-estate) costly. (rule of thumb for Si predriver area : $1W/mm^2$)
  - Driving SiC at high frequency without Rgate is at the edge of what is commercially appealing.
  - Driving GaN at high frequency can (power wise) be done without Rgate.
- For 1.2kV GaN and SiC : in practice, **gate-source inductance requires dI/dt** to be limited, so they are driven with Rgate

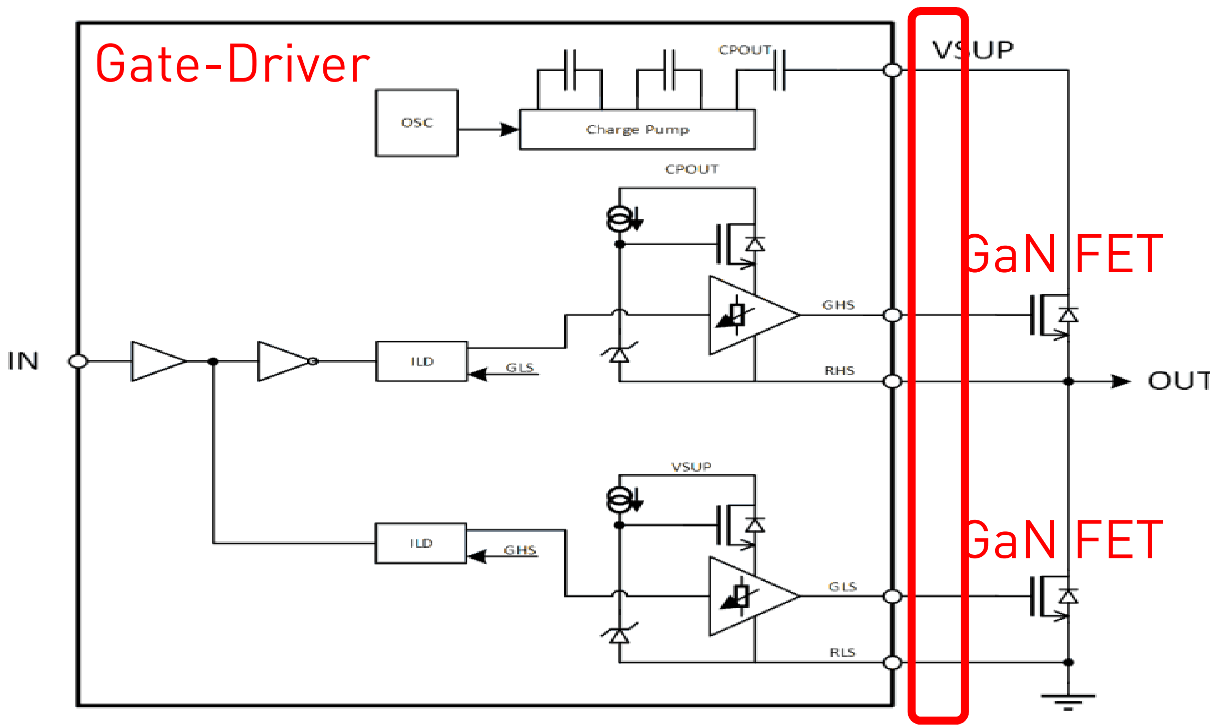
Rgate trade-offs

- Pull-up:
  - Limit the dissipation inside the gatedriver (Pgate /2)
  - As fast as possible,
    - limited excessive ringing of outputs/supply nodes
    - gate-source loop inductance / ringing / overvoltage
  - Typically iterative design
- Pull-down:
  - Limit the dissipation inside the gatedriver (Pgate/2)
  - Keep the gate tied down to the source as good as possible (or negative potential) ←→ parasitic turn-on
  - For inductive loads, a non-zero pull-down may be used to control the output dV/dt, but a miller clamp is required!

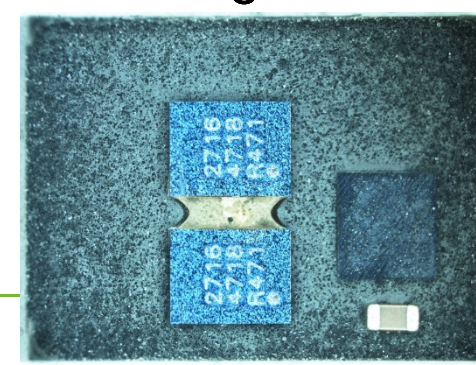
Challenges in Driving GaN Gates

HOW NOT TO DO IT

1. Main GaN advantage = Switching Speed. Excess Gate-Loop Inductance/Length kills performance.



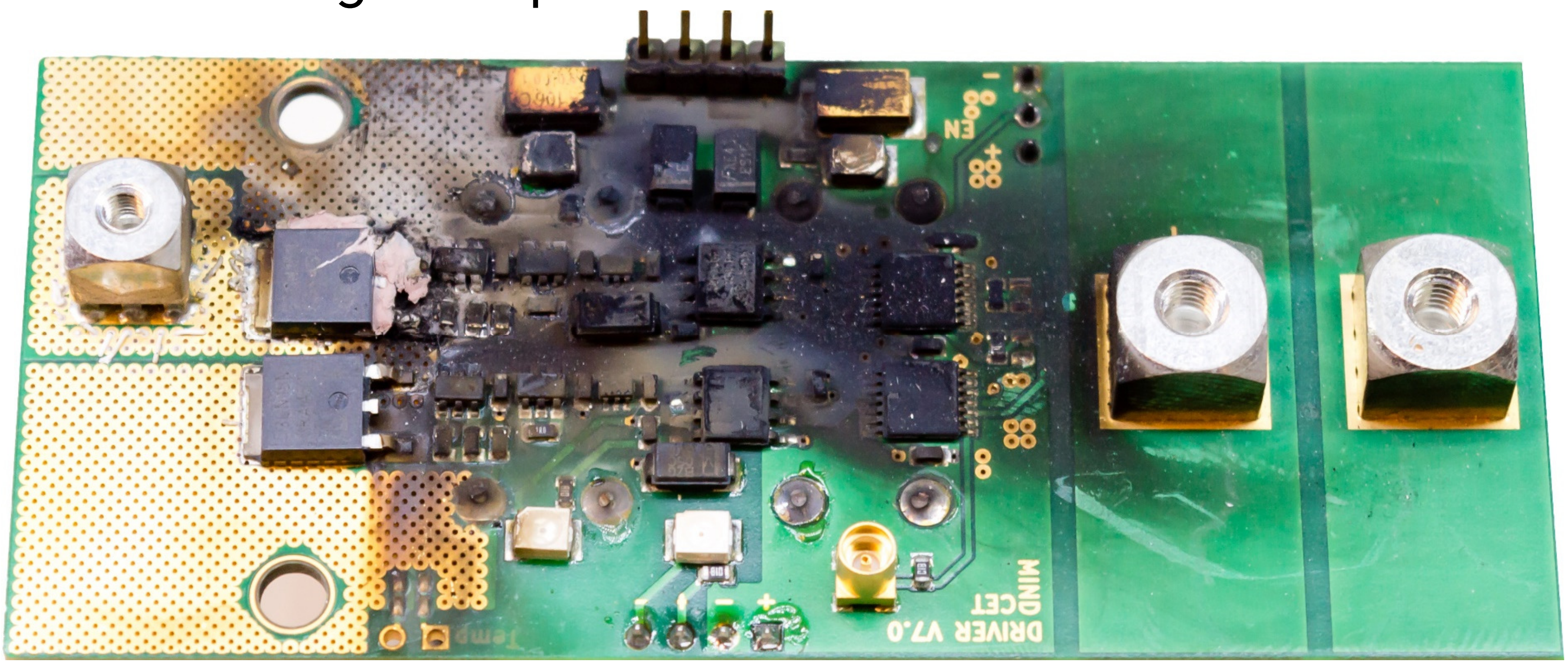
- Driver Package
- PCB layout
- GaN Package
- Temperature constraints for the gate-driver



Driving GaN Gates

HOW NOT TO DO IT

2. High dV/dt & low Cg/Cdg ratio = Parasitic Turn-on. Many SPMS designers have seen their first trials with GaN resulting in expensive fireworks.



Challenges in Driving GaN Gates

HOW NOT TO DO IT

3. Extreme dV/dt (100V/ns and more) = problematic for Reliable Gate-Driver Operation.

4. The Delay Matching of the Gate Signals of a half-bridge circuit is crucial for its reliable operation. This requires Accurate Dead-Time Generation and HS/LS Delay Matching. Nano-second precision is required!

Challenges in Driving GaN Gates

HOW NOT TO DO IT

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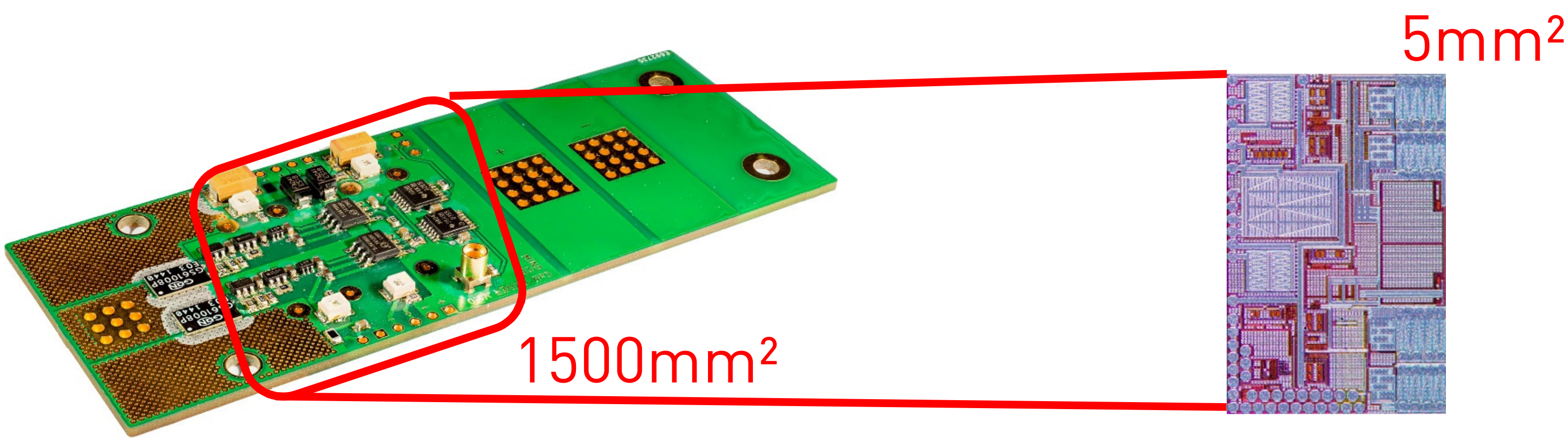
5. Gan Vgate = ca. 4-7V. MOSfet drivers support ca. 8-20V. Accurate and Adapted Gate-Drive Voltage needed. Overvoltage is problematic.

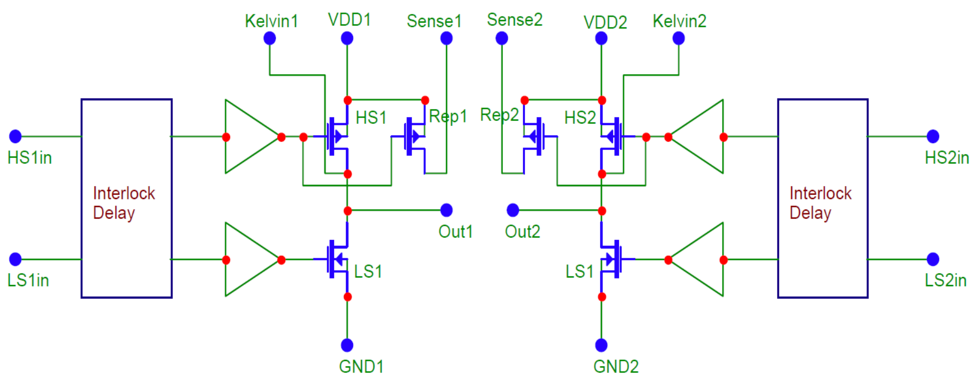
6. Maximize Integration by minimizing external components = Highest Power Density.



High-Speed LS GaN Gate-Driver

HOW TO DO IT RIGHT: MDCD073

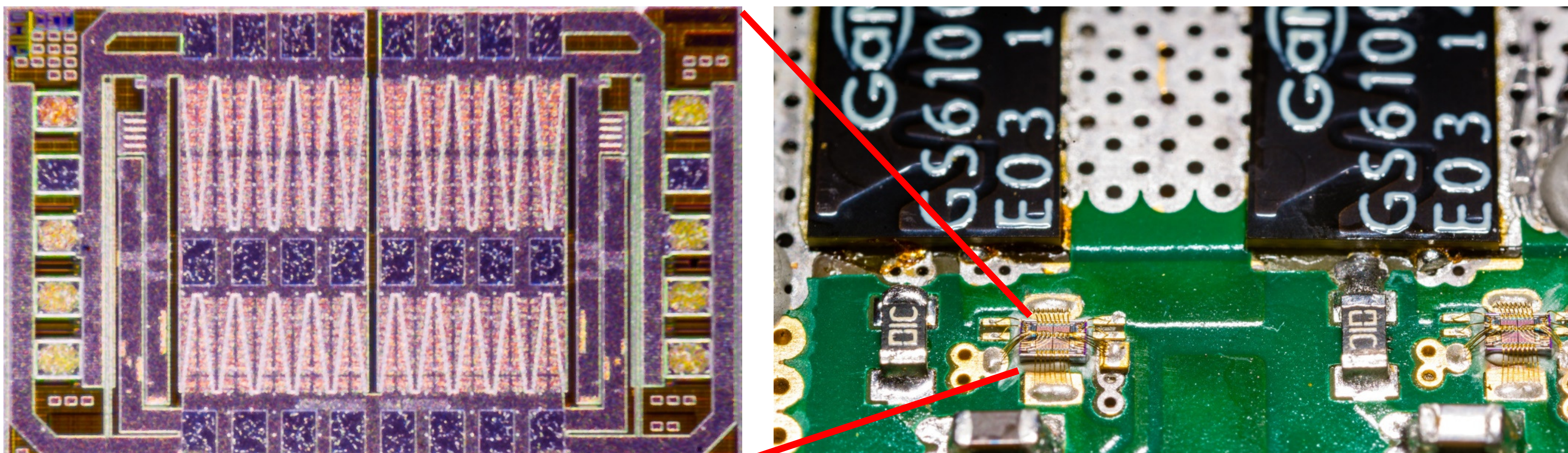
- Dual Half-Bridge
- Ron_LS = 150mOhm
  => No Parasitic Turn-On
- Ron_HS = 240mOhm
  => Fast Drive
- Output rise/fall-time = 500ps
- 7-2.5V operation, 4A peak
- Ultra Low Inductance Lay-Out
- 0.9mm^2



High-Speed LS GaN Gate-Driver

HOW TO DO IT RIGHT: MDCD073

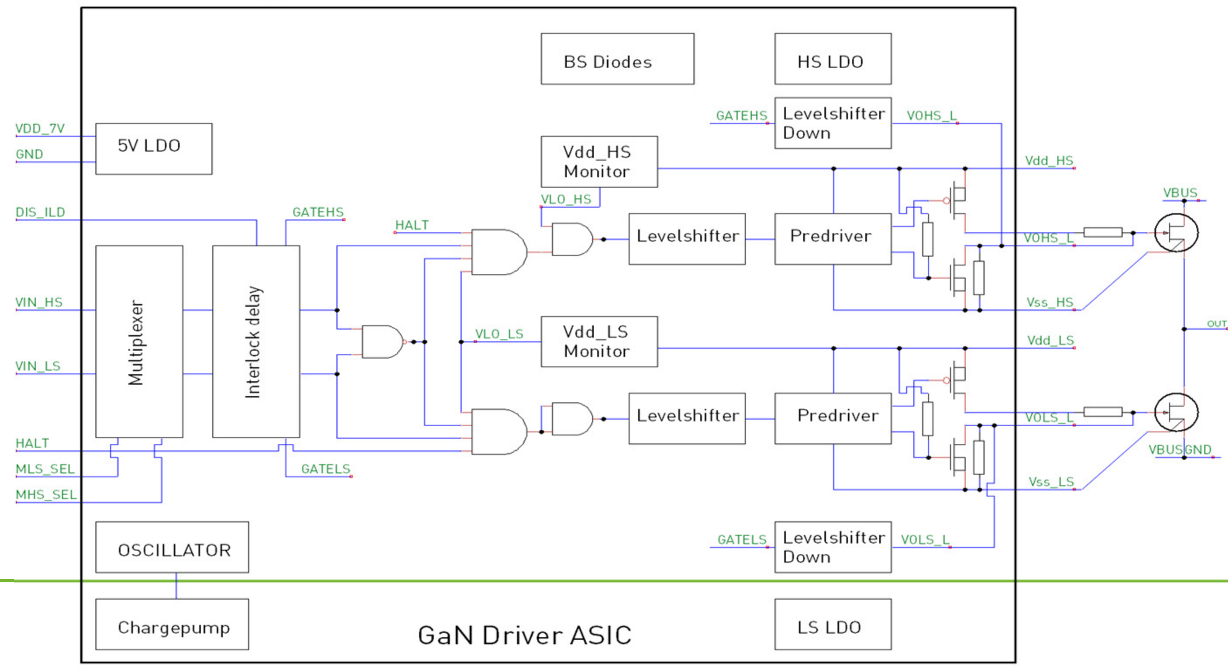
- CoB approach for shortest gate-loop
- Nanosecond gate-drive possible
- 10x improvement over commercial drivers
- Discrete level-shifting limits dV/dt to about 20V/ns



High-Speed HS/LS GaN Gate-Driver

HOW TO DO IT RIGHT: MDCD074

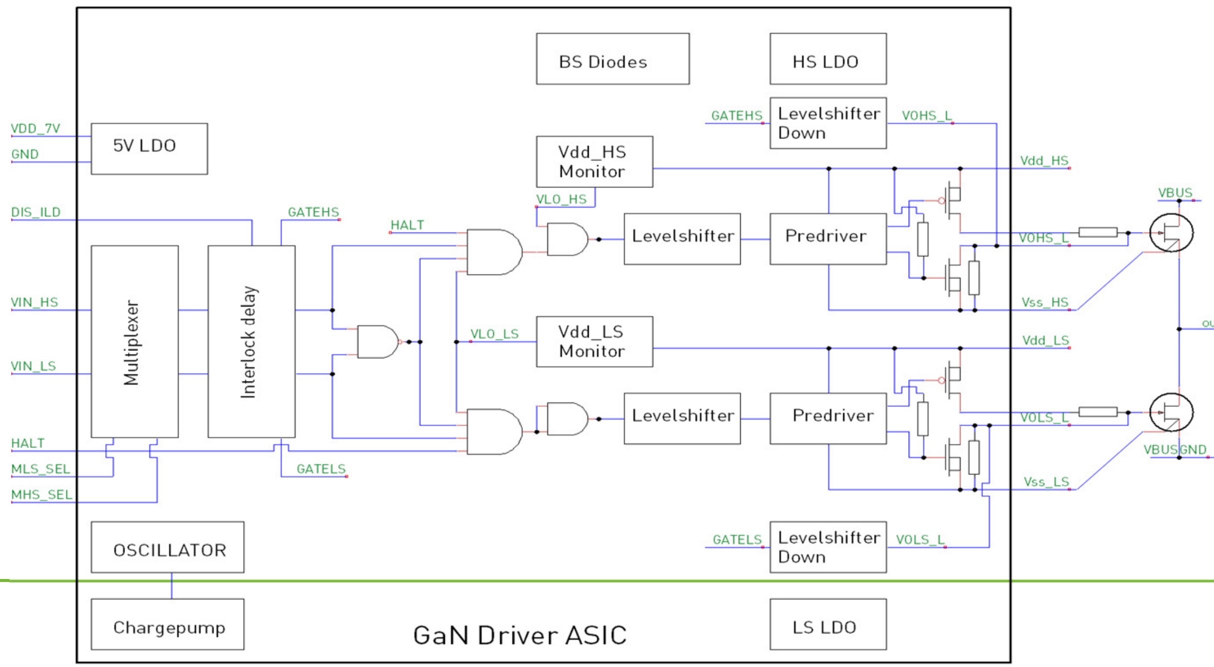
- Floating High-Side up to 100V
- Integrated Level-Shifters
- Integrated Bootstrap
- Integrated Charge-pump (100% duty, start-up...)



High-Speed HS/LS GaN Gate-Driver

HOW TO DO IT RIGHT: MDCD074

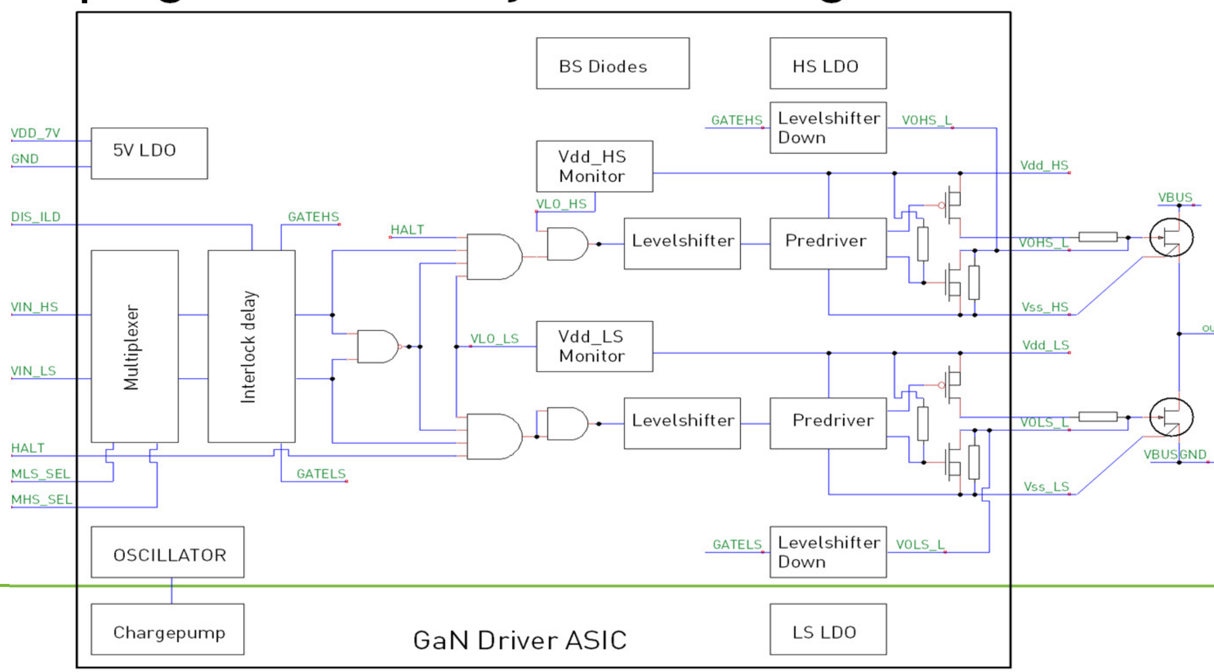
- Integrated Automatic Dead-Time
- Gate-Voltage Monitor
- Integrated floating supplies
- Buck/Boost mode
- Synchronous/Asynchronous mode



High-Speed HS/LS GaN Gate-Driver

HOW TO DO IT RIGHT: MDCD074

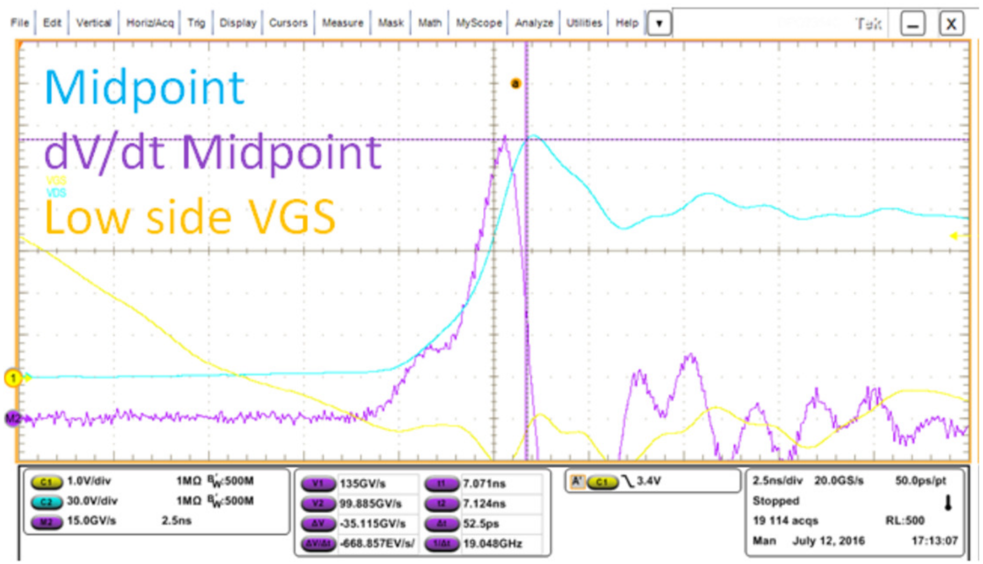
- Gate Voltage 4-10V
- Gate rise/fall-time <1ns
- HS/LS propagation delay 10ns
- HS/LS propagation delay matching <1ns

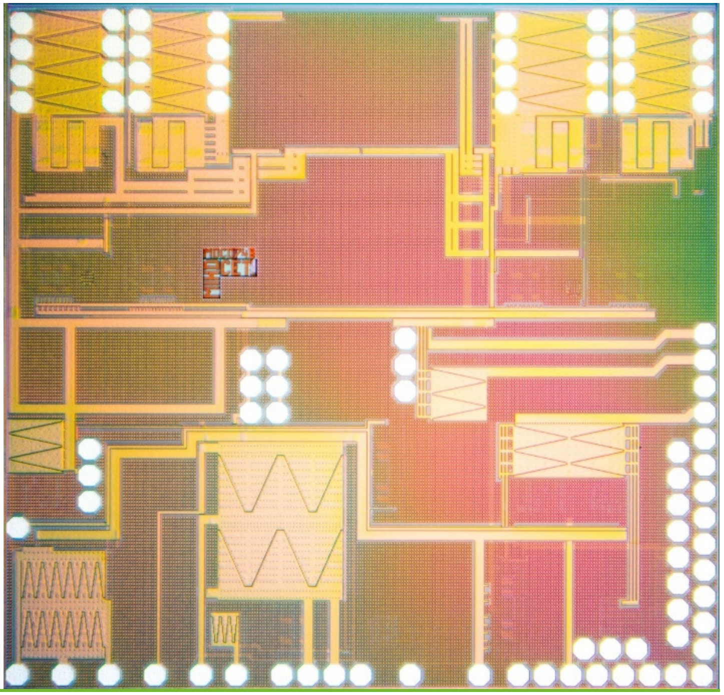


High-Speed HS/LS GaN Gate-Driver

HOW TO DO IT RIGHT: MDCD074

- CoB approach for optimal gate-loop
- >100V/ns dV/dt tested!!!
- 100V floating capability
- -55°C to 175°C temperature range!





Putting it all into A MODULE

HOW TO DO IT RIGHT: GaNyMAD

"Abduction of GaNyMedes" (1611)

By Pieter Paul Rubens

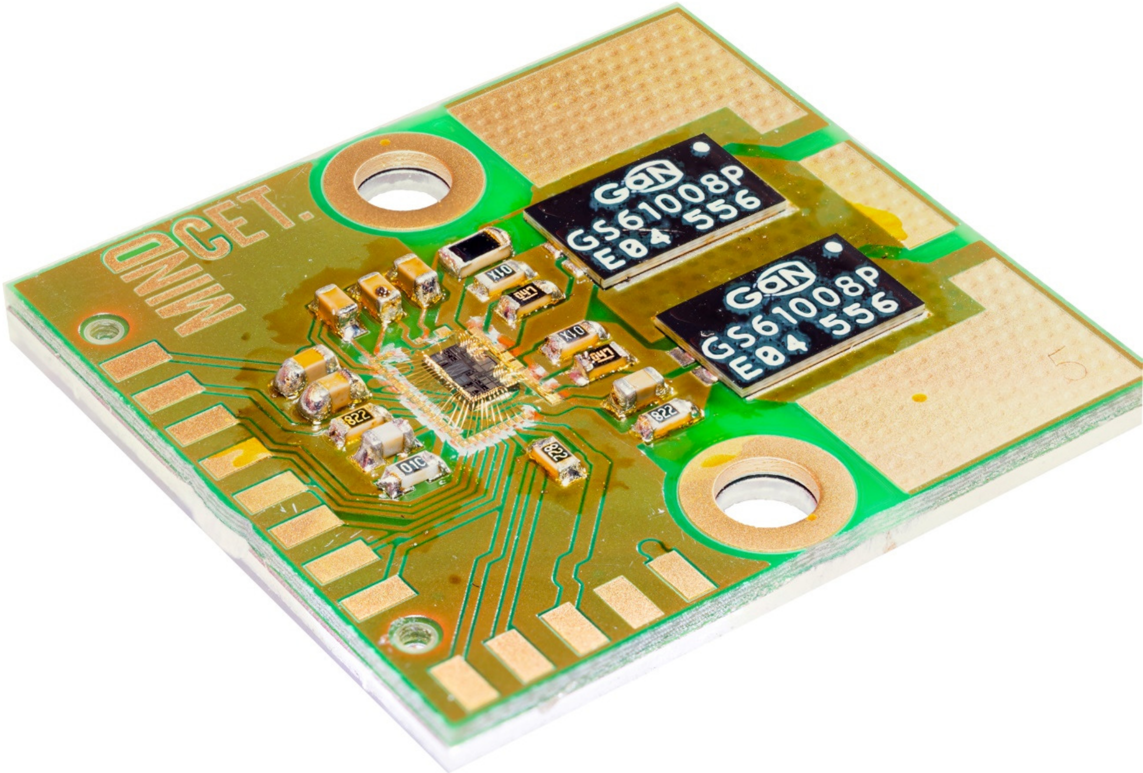
"Production of GaNyMAD" (2017)

By MinDCet

Putting it all into A MODULE

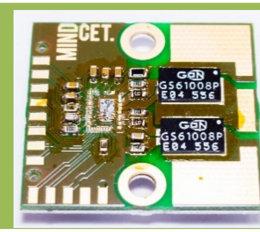
HOW TO DO IT RIGHT: GaNyMAD

- Alu-core PCB with CoB
- Allows for optimal thermal design
- 100V/90A GaN Half-Bridge
- 26x28mm² footprint
- 14x22mm² core
- Power C & L external
- User needs to provide logic signals and don't worry about gate-drive!!!



GaNyMAD vs LM5200

Pure powerstage comparison

		
Peak power	100V @ 90A	80V @ 10 A
Average output power [W]	4500	400
Additional external comp.	0	12
Core area [mm²]	308	48 + 89 (ext components)
Power density [W/mm²]	14.6	3.41
Dead-time generation	Internal	External
Propagation delay	10ns	30ns
100% duty cycle	Yes, internal chargepump	No
Cost / Pout [EURcent/W]	1	2.2

The new GANYMAD Power Module

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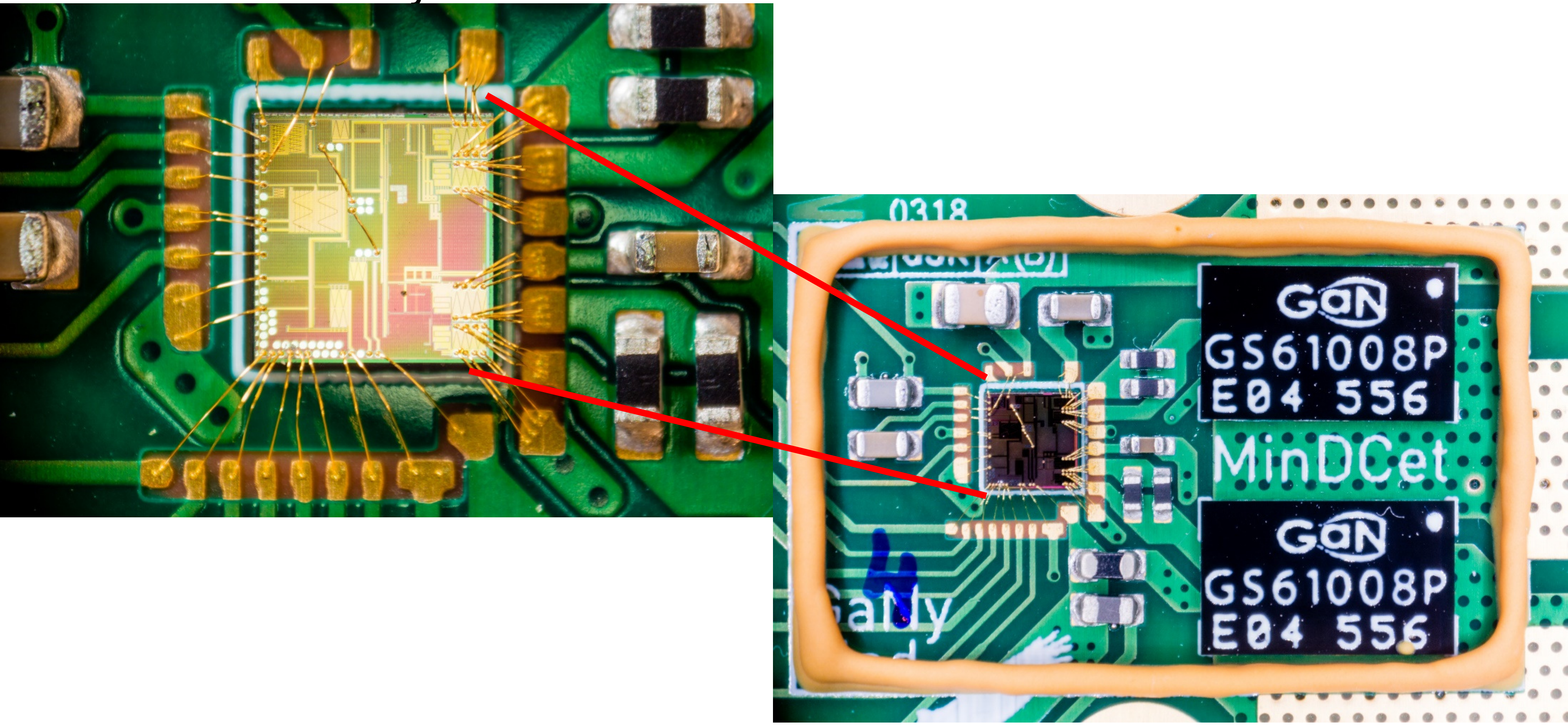
- Functionally tested in a brand-new GANYMAD module

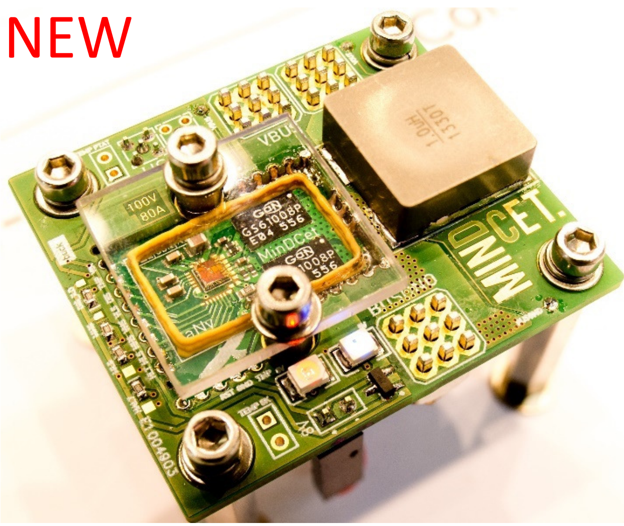


The new GANYMAD Power Module

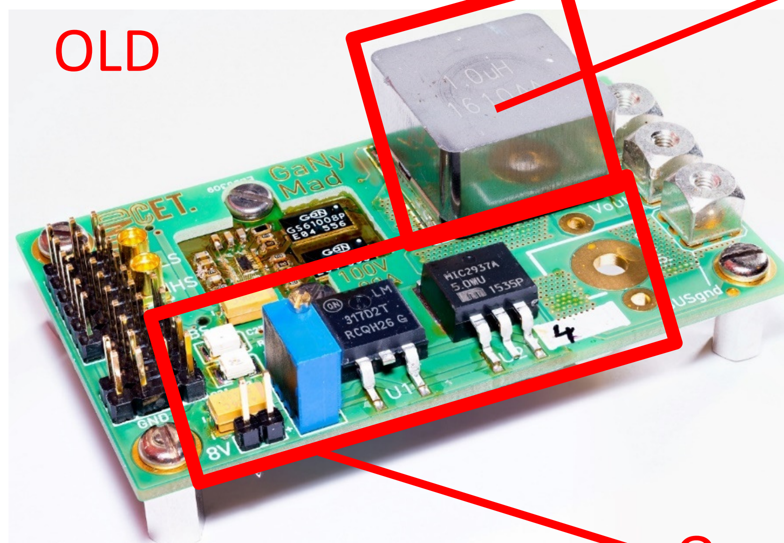
System-level Impact

- Reduce # external components in the system
- Improve speed

NEW



OLD



Higher Speed = Smaller Output Filter: 50% size reduction

On-chip regulators, No need for external ones

The new GANYMAD Power Module

Efficiency measurements

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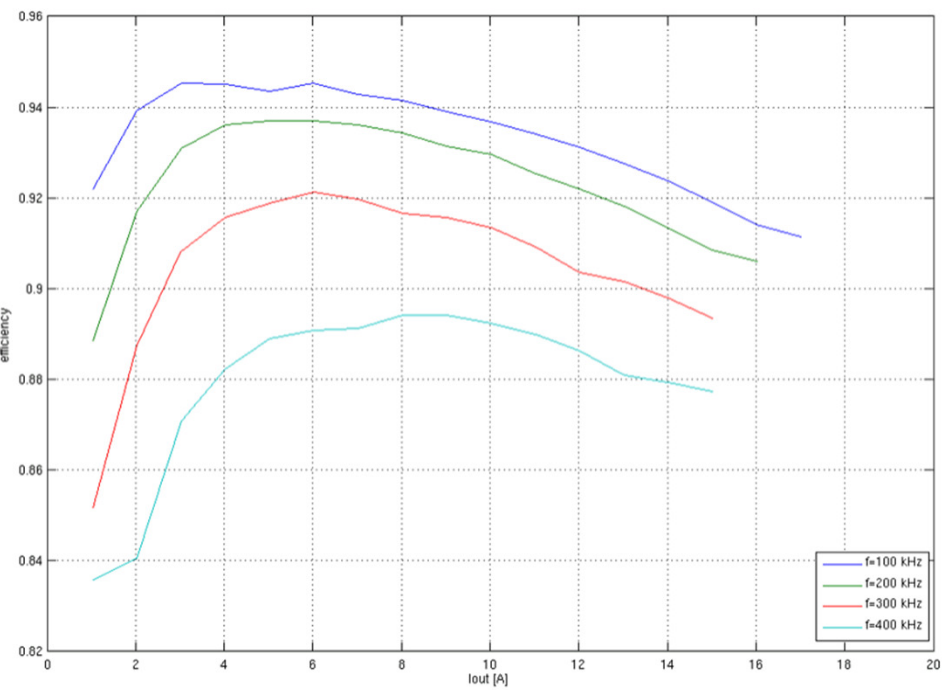
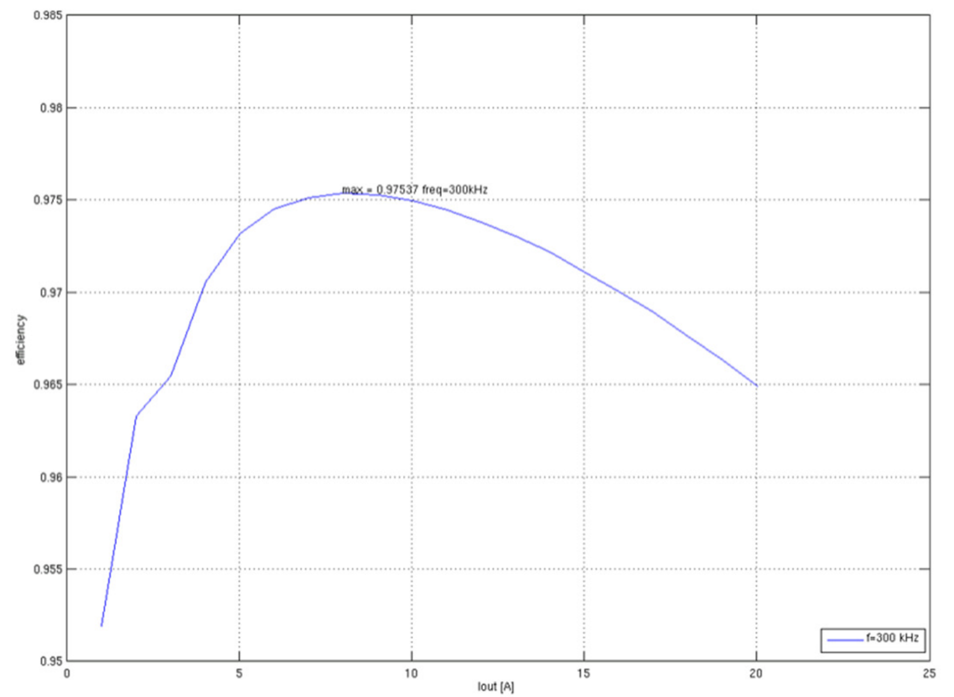
48V to 3V3 buck mode, n_{eff} = 94.5%



48V to 12V buck mode, neff = 97.5 %



Conclusion on GaN Driving

- Getting the maximal performance out of GaN requires a custom gate-driver
- Neglecting one of the aspects (gate-loop, parasitic turn-on…) will result eventually in failure
- The optimal solution combines speed with high-drive strength
- You need to integrate the gate-driver system to cope with the high dV/dt of the output node
- A complete Module gives the user peace-of-mind and first-time right succes for integration

SiC Driver requirements

Spec :

- SiC FETS with Qg = 3uC , switching at 50kHz, dVgs = 25V ➔ Pg = 3.75 W
- 12A charging current of the gate
- Propagation distortion < 20 ns (symmetric for turn-on and turn-off)

First observations:

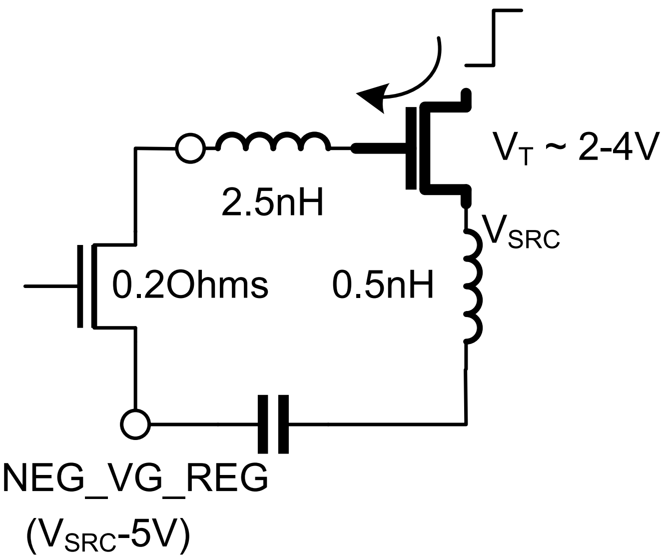
- Pg cannot be (economically) burnt in the driver IC => external gate resistors are required.
- There is a need for miller clamping => 2 pulldown drivers are needed
  - 1 for gate discharge
  - 1 for miller clamping

Driving SiC gates

- Tight control of overdrive voltage is needed
  - Sensitive to oxide breakdown (Vgs << Vbd)
  - SiC acts as a voltage controlled resistor (weak saturation) (Vgs >>)
- Negative steering of gate during turn-off is required
  - Poor control of gate-source impedance (resistive and inductive) ←→ discrete GaN transistors
  - Cdg can easily cause several volts of overshoot during Vds transient => miller clamping is a must

Miller clamping

- Vmc = 4V
- Vlgs = 2.5V
- Vth = 2...4V ...



$$\frac{\Delta V}{L} = \frac{dI}{dt} = \frac{20A}{20ns.nH} = \frac{1V}{nH}$$

MinDCet SiC driver implementation

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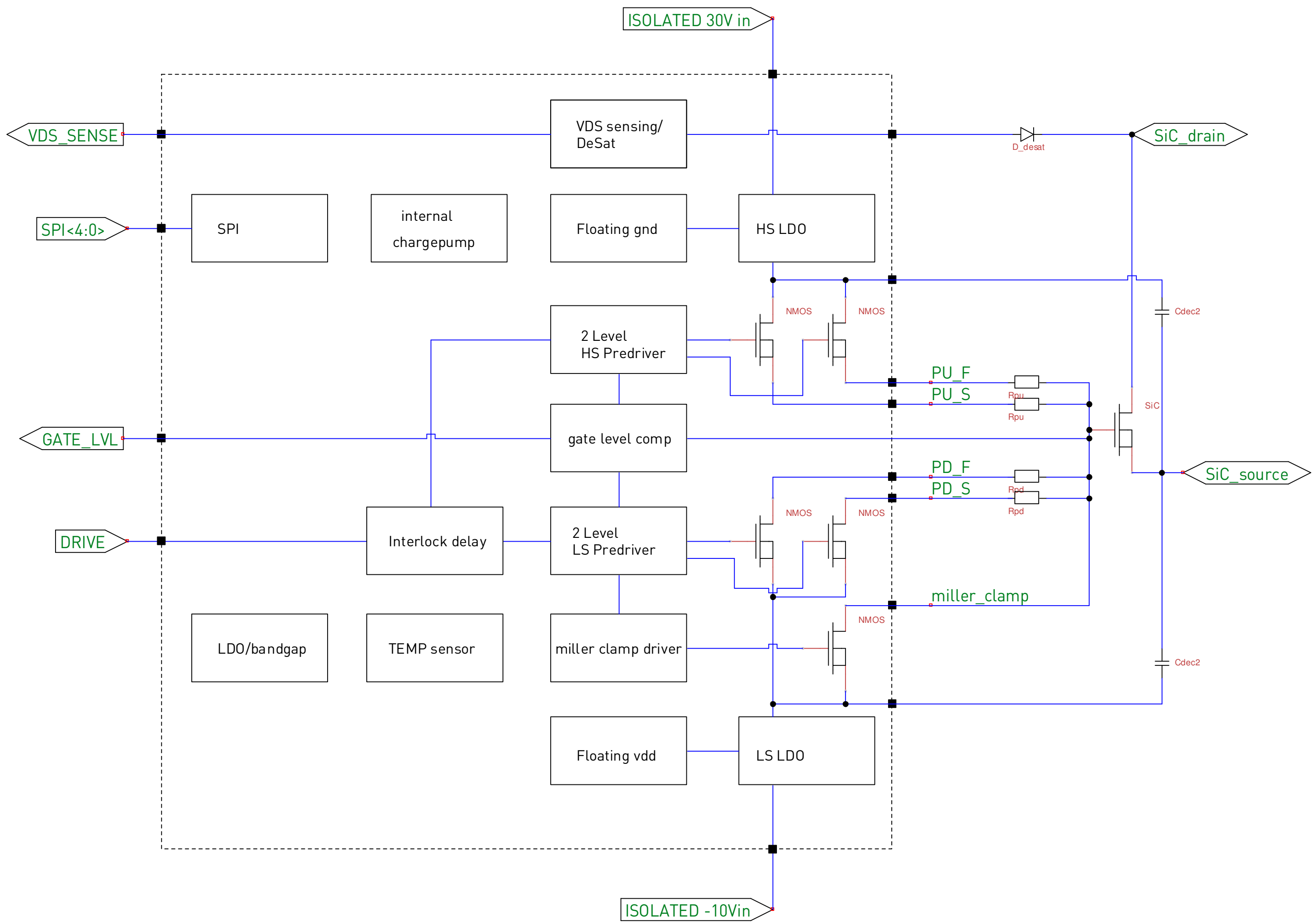


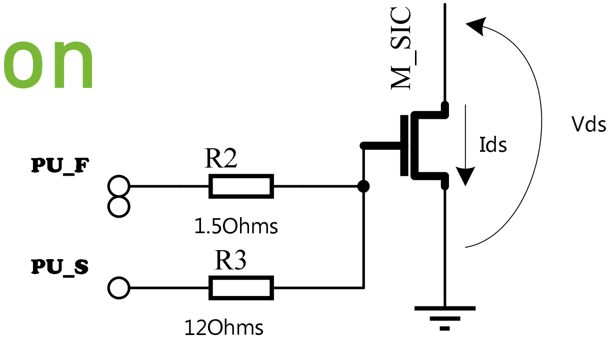
SiC driver features

- Programmable LDOs for better Vgs,on control
  - Waste of power ➔ dropout over HDO has to be minimal
- Selectable 2 phase turn-on/off
- Self latching Miller clamp
- DESAT detection
  - Fast overcurrent detection is required.
  - $t_{shortcircuit,SiC}$ <= 1us ⇔ $t_{shortcircuit,igbt}$ <= 10us
- Gate comparator for gate level monitoring or protection

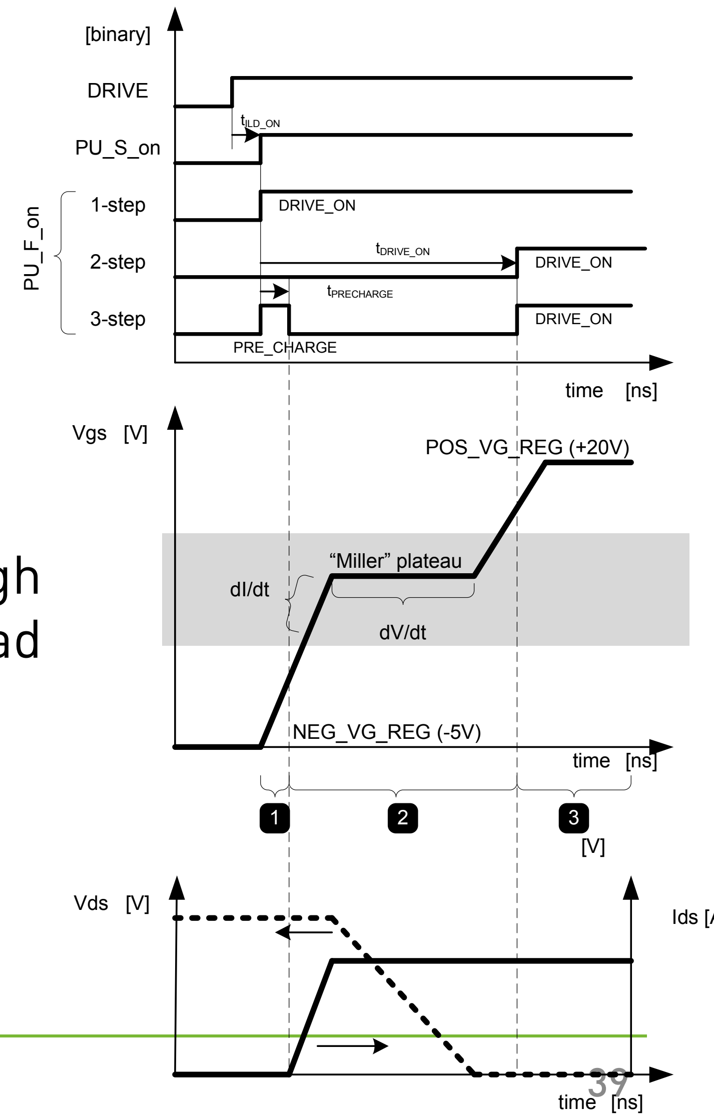
Multiphase turn-on/off?

- Rationale:
  - Keep the dV/dt under control (separate charging path)
  - speed up charging of the gate after the miller plateau to reach nominal Rdson * I^2 ASAP
  - Clamp the SiC gate to the source when it needs to be off.
- Combine EMI (limited dV/dt and dI/dt) control with fast turn-on/off
- Allows larger dutycycle ranges and shorter non-overlap delays

SiC gate turn-on

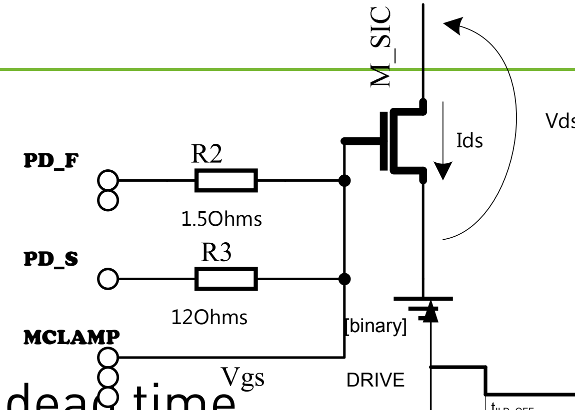


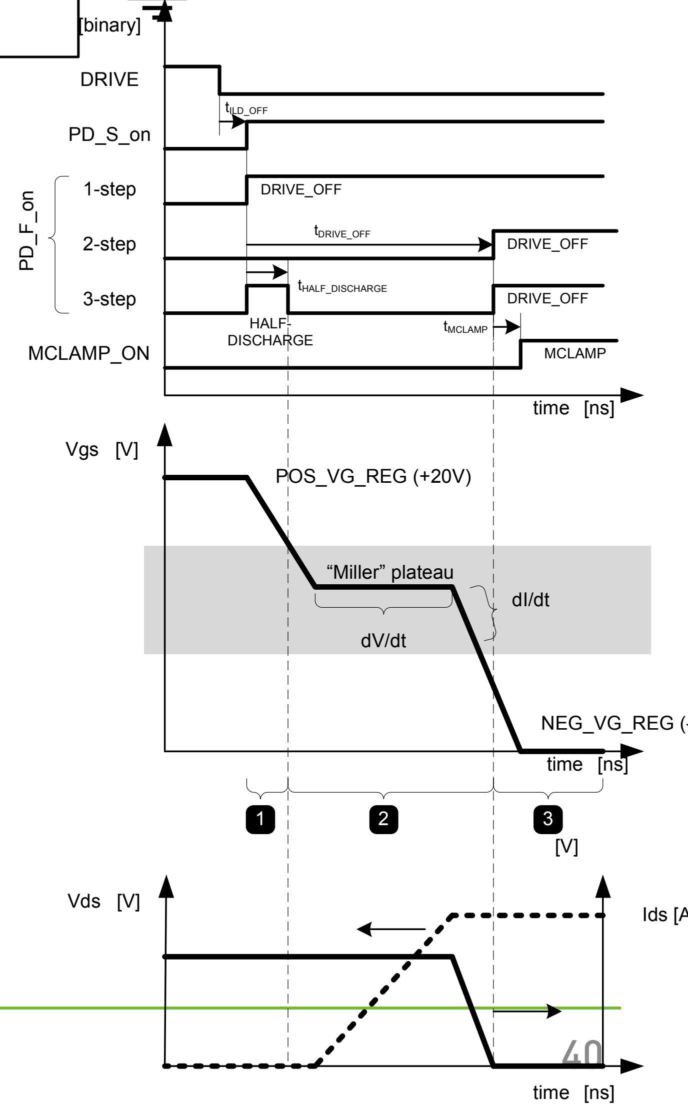
- Always
  - PU_S turns on after IC turn-on dead time
- 1-step
  - PU_F turns on after IC turn-on dead time
- 2-step
  - PU_F turns on with prog delay or through gate comparator after the IC turn-on dead time
- 3-step
  - Not implemented



SiC gate turn-off

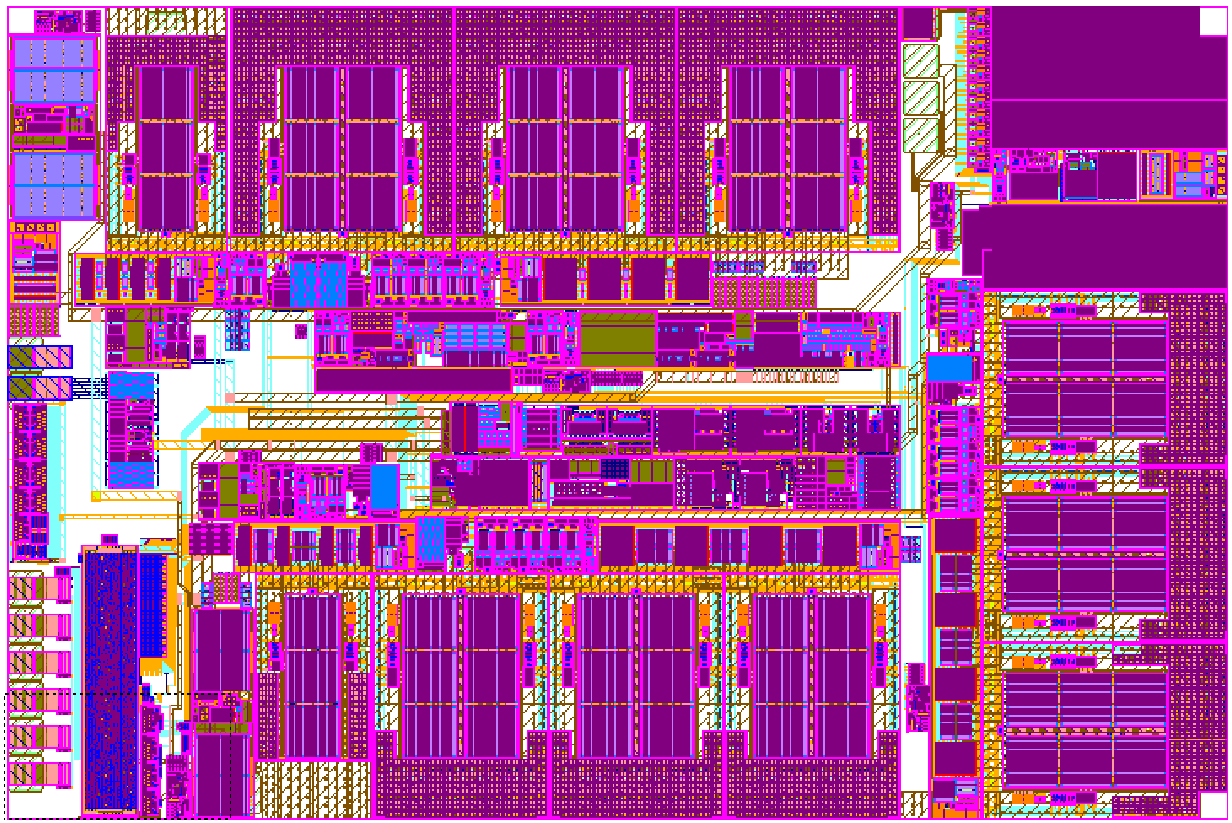
- Always
  - PD_S turns on after IC turn off dead time
- 1-step
  - PD_F turns on after IC turn off dead time
- 2-step
  - PD_F turns on with prog. delay or through gate comparator after the IC turn off dead time
- 3-step
  - Not implemented
- Miller clamp turns on after prog delay or self latching after DRIVE_OFF





Fab out = this week

- Characterization planned Nov 2018



Challenges in SiC design

- There is a large distance between the upper gate-source connection and the lower gate-source
  - Gate driver / PCB impedances can be well controlled ⇔ module impedances
  - What is the module GS loop inductance, and how is it distributed ?

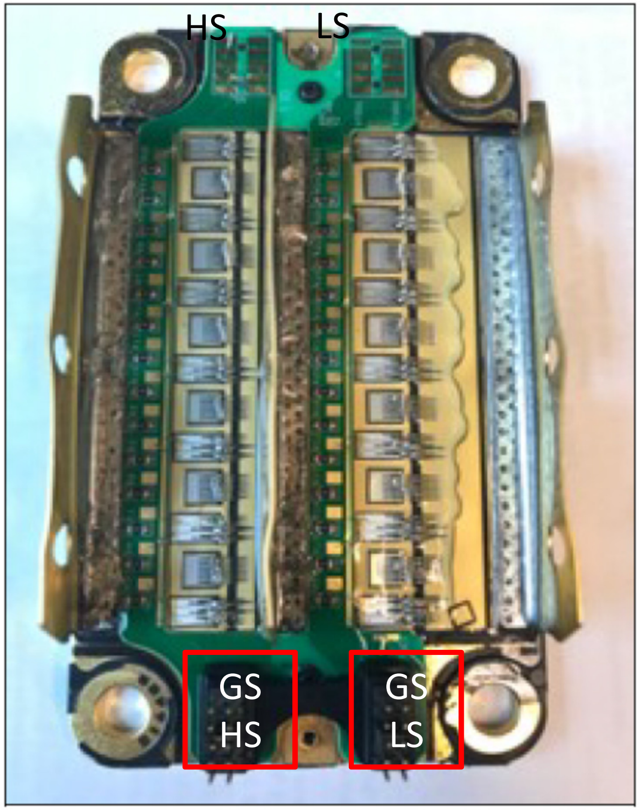
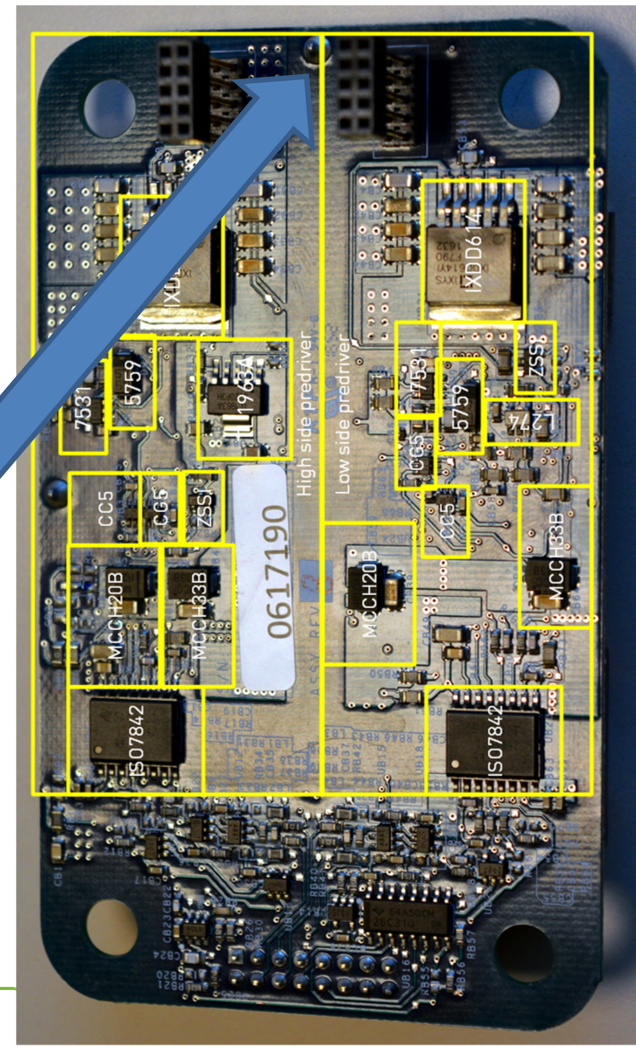


Fig. 1. Internal layout of the 1.2 kV module.

Source: Estimation and Minimization of Power Loop Inductance in 135 kW SiC Traction Inverter, APEC Aberg et al 2018

Challenges in SiC design

Source : CreeCGD15HB62LP Predriver board



- A fast gate driver does not mean a fast SiC inverter
  - Lots of parasitic inductances involved – typically the manufacturer will advise to not drive it too fast…
- PCB design of the gate driver will be key
  - Keeping the gate-source loop low inductive
  - **Better** : integration of the predriver in the power module !

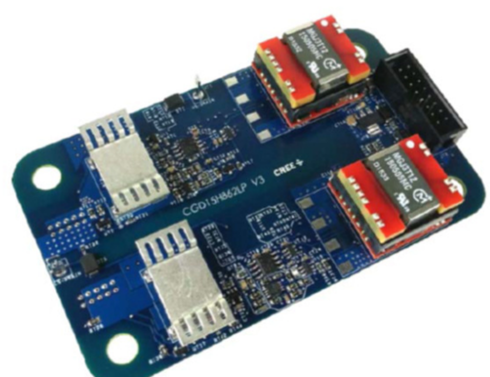


Figure 4. Wolfspeed's high performance gate driver.

SiC modules, future outlook

MINDCET. Custom Integrated Power Management Solutions

- Lamination of busbars reducing bus inductance

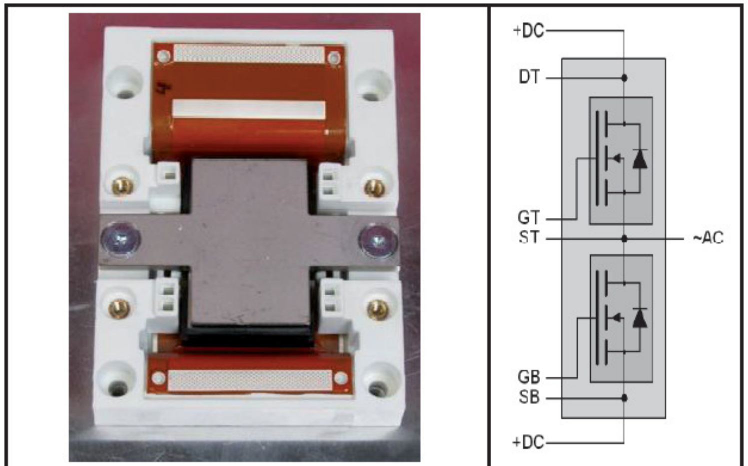


Fig. 3: Photo of 1200 V / 400 A SiC-MOSFET half bridge module assembled in both side sinter-technology (SKiN); one switch has 8 x 50 A MOSFET in parallel; module size is 69 x 92 mm

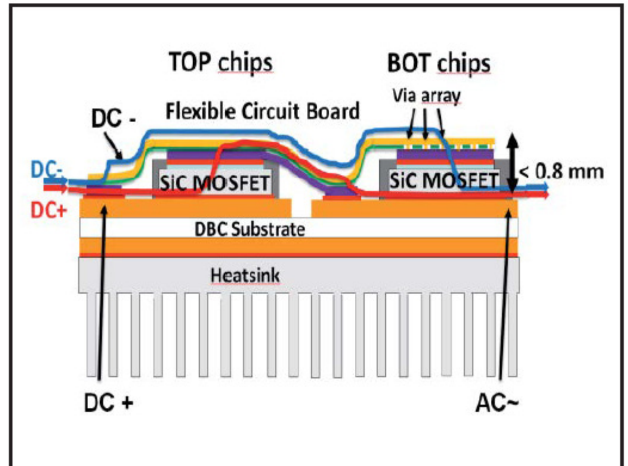


Fig. 4: Cross section of the module and simplified demonstration of the commutation loops of the very low inductive design

Source : **High power, high frequency gate driver for SiC MOSFET modules, Semikron, PCIM 2016**

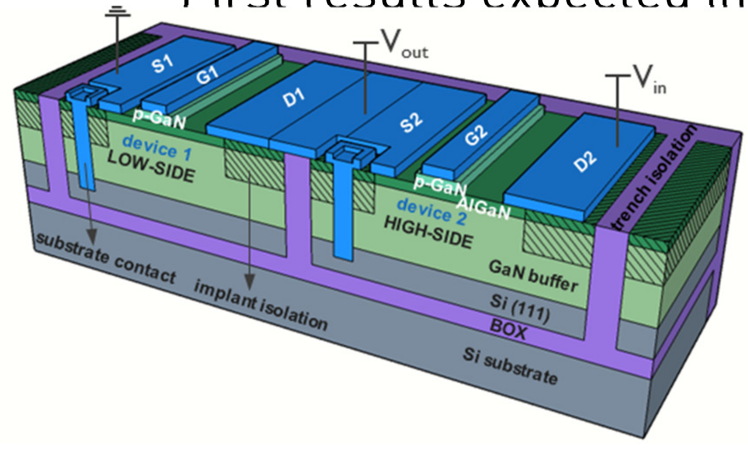
Conclusion on SiC Driving

- Getting the maximal performance out of SiC requires a custom gate-driver
- Performance of gate driver is limited by physical assembly of the SiC module
- Future improvements:
  - Mechanical
    - Laminated power module connections
    - Laminated gate-source connections
  - Electrical
    - Integration of the gate driver inside the module

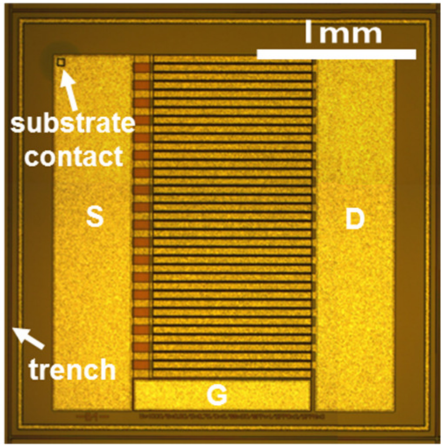
What holds the future?

Driving wide-bandgap to the limits !

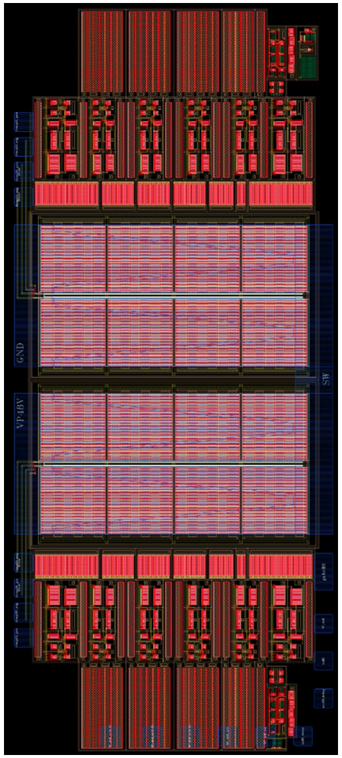
- First GaN-on-SOI 100V halfbridge with integrated predrivers *
  - Tape out Oct 2018
  - First results expected in Q1 2019



Schematic cross-section of GaN-on-SOI structure, featuring buried oxide, oxide filled deep trench, local substrate contact and p-GaN HEMT devices. Picture courtesy IMEC.



Optical microscope picture of p-GaN HEMT on SOI with deep trench isolation and local substrate contact. Picture courtesy IMEC.



Floorplan of the symmetrical GaN-on-SOI 32 mOhm/10A halfbridge

* SloGaN project : https://www.imec-int.com/en/what-we-offer/research-portfolio/slogan

What can we do for you?

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