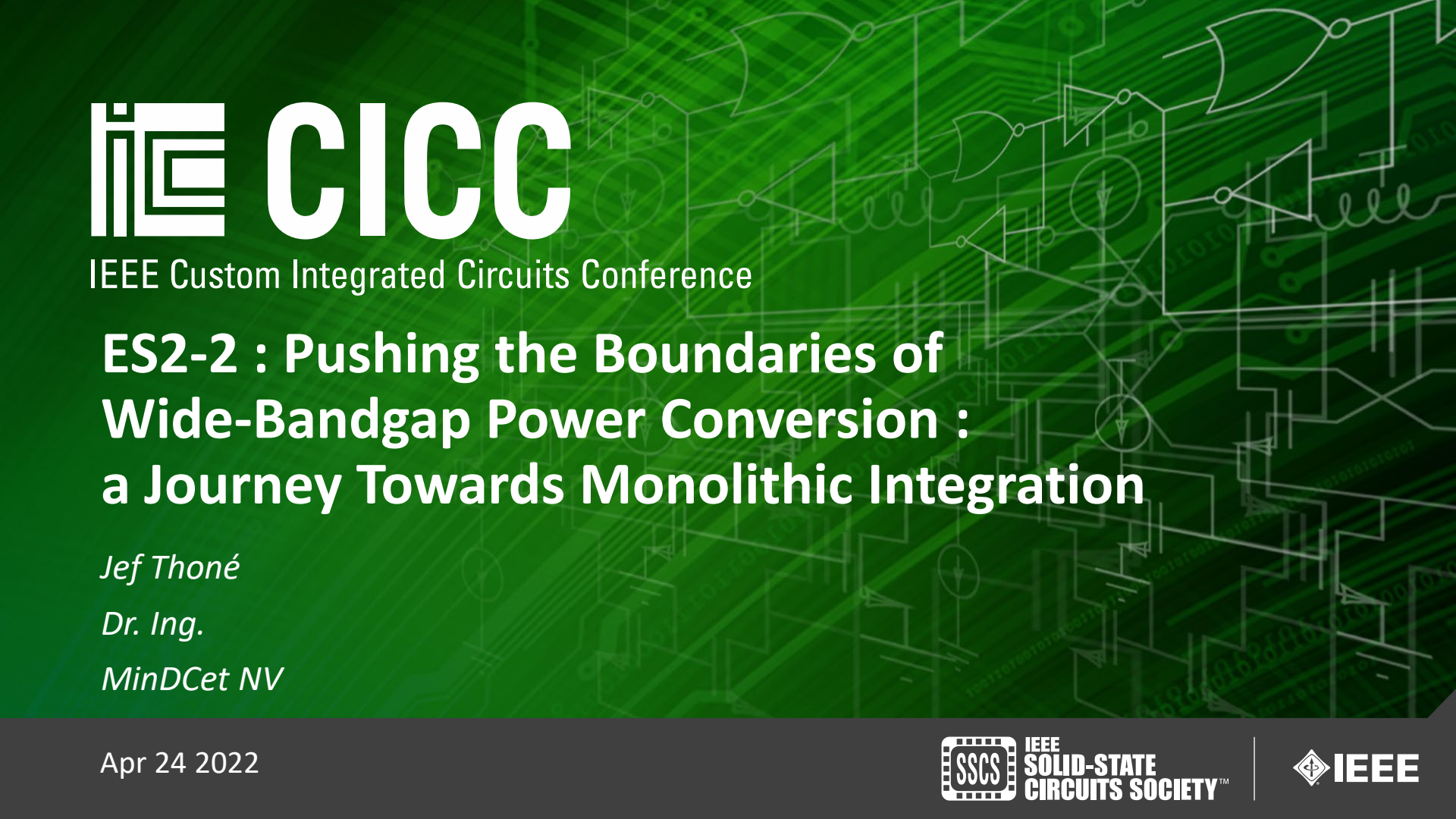

ES2-2 : Pushing the Boundaries of Wide-Bandgap Power Conversion : a Journey Towards Monolithic Integration

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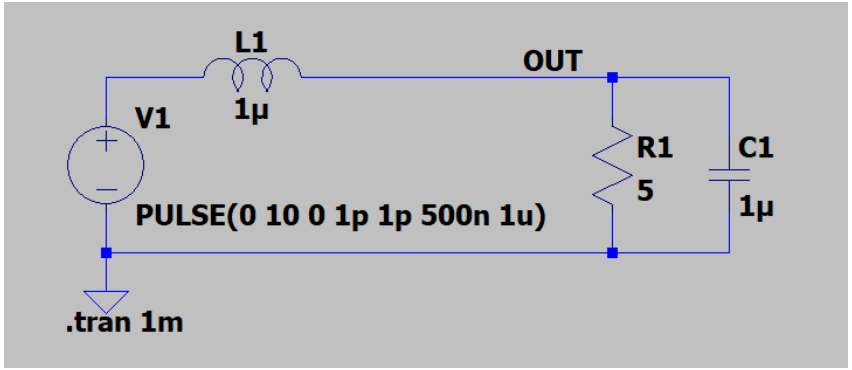
- Introduction
- On capacitance and charge
- Challenges when driving GaN
- Path towards monolithic GaN

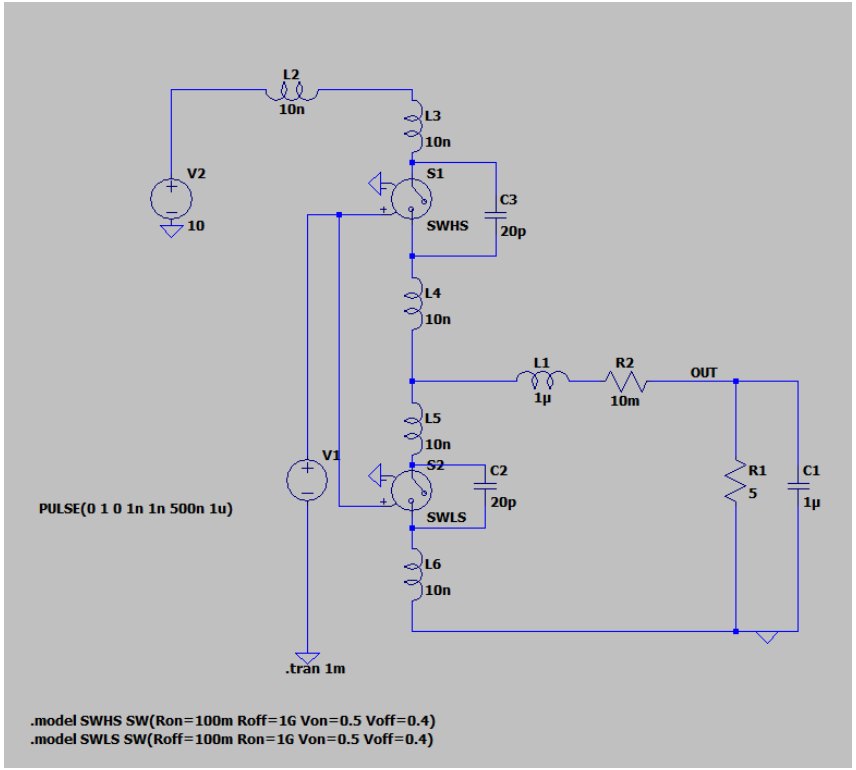
Power conversion: what do we want ?

- Move energy from a source to a load at 100% efficiency
  - Switching infinitely fast at zero impedance with zero power loss
  - Intermediate storage into a lossless capacitor or lossless inductor
  - No parasitic capacitance / inductance or losses
- How : 99.9% efficient converter (only in LTspice land)



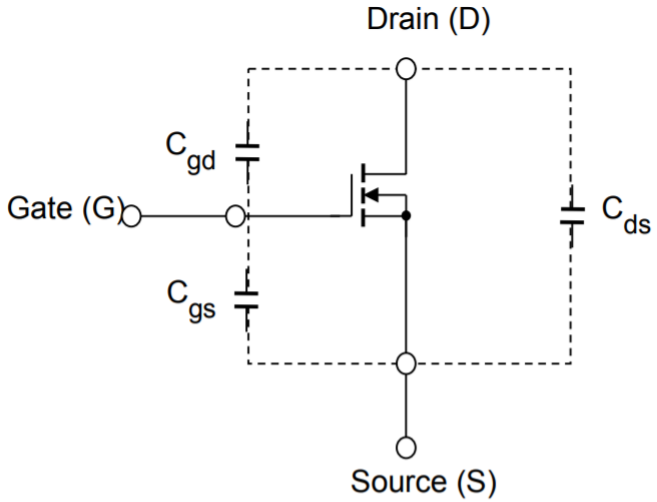
What do we get?

- Lossy inductor
  - Core losses
  - Winding losses
- Lossy capacitor
  - ESR
  - Dielectric losses
- Lossy switches
  - Finite switching times
  - C_{oss} losses
  - Reverse recovery
  - Finite switching resistance
  - Non-overlap delay
  - Parasitic capacitance
  - Parasitic inductance



Transistor capacitances re-cap

- C_{iss} : defines gate switching losses
- C_{oss} : defines output switching losses
- $C_{rss} = C_{gd}$
- Non-linear capacitances vs drain-source or gate-source



Input capacitance $(C_{iss}) = C_{gd} + C_{gs}$

Output capacitance $(C_{oss}) = C_{ds} + C_{gd}$

Reverse transfer capacitance $(C_{rss}) = C_{gd}$

Definitions of charges : JEDEC standard 24-2

- $Q_{gs,th} = C_{iss} * V_{gs,th}$
- $Q_{gs} = C_{iss} * V_{gs,pl1}$
- $Q_{gd} = C_{gs} * (V_{gs,pl1} - V_{gs,pl2}) + \int C_{dg}(V).dV_{ds}$
- $Q_g = Q_{gs} + Q_{gd} + C_{gs} * (V_{gs,pl2} - V_{gs,pl3})$

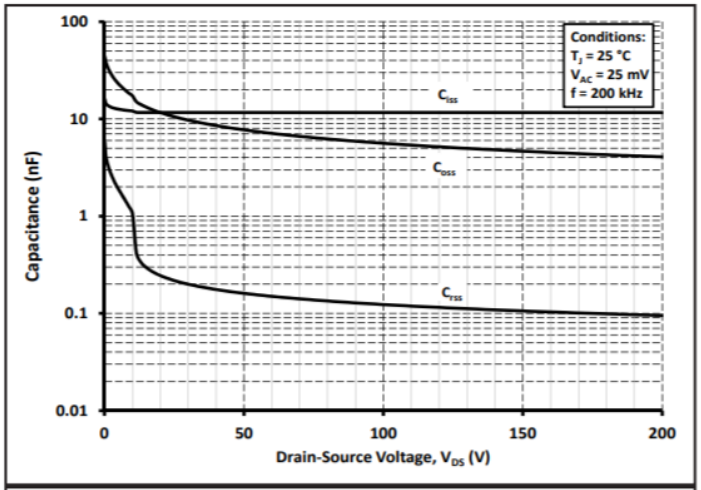
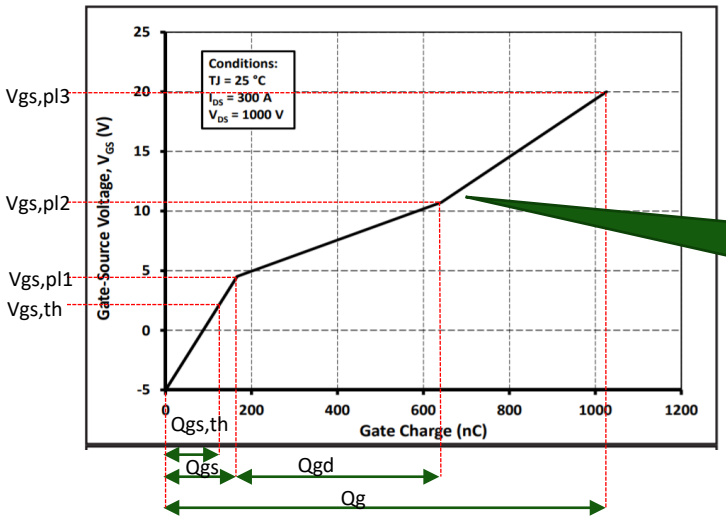


Figure 16. Typical Capacitances vs. Drain-Source Voltage (0 - 200 V)

REF: CAS300M12BM2 datasheet

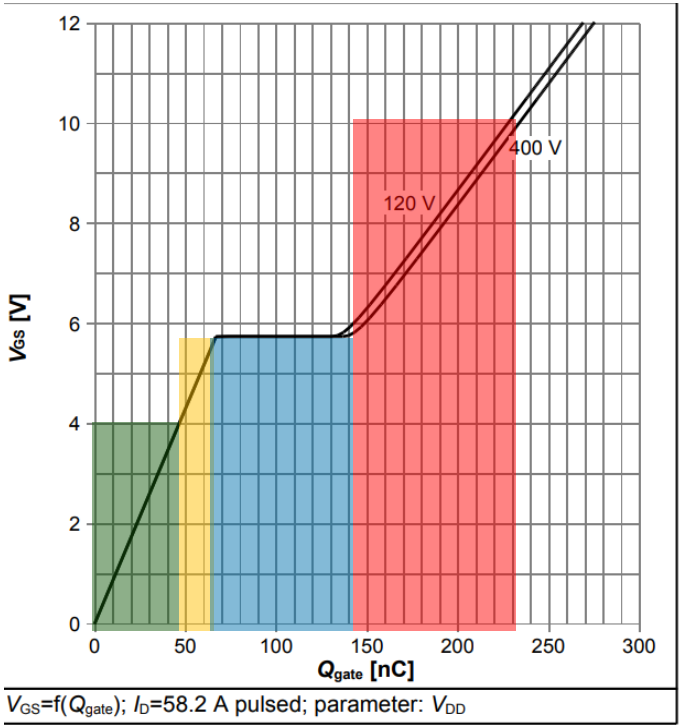


How to interprete this?

- $Q_{gs,th}$: Vds = VBUS
  - Charging Cgs ➔ Vth
  - Charging Cdg @ offstate ➔ Vth
- $Q_{gs,pl}$: Vds = VBUS
  - Charging Cgs ➔ Vth + Vdsat
  - Charging Cdg @ offstate ➔ Vth + Vdsat
- Q_{gd} : Vds = discharging to 0V
  - Vgs is balanced with decreasing Vds ➔

  Cgd discharges until Vgd = Vgs according Crss
  - When Vgd < Vgs

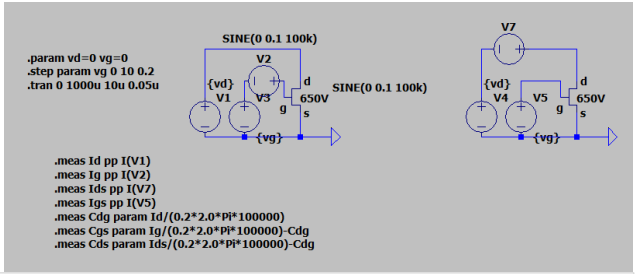
  Cgd discharges until Vgd = - Vgs according to Crss
- $Q_{gs,pl}$ => $Q_{gs,max}$: Vds = +- 0V
  - Further charging of Cgs + Cgd until gate drive level



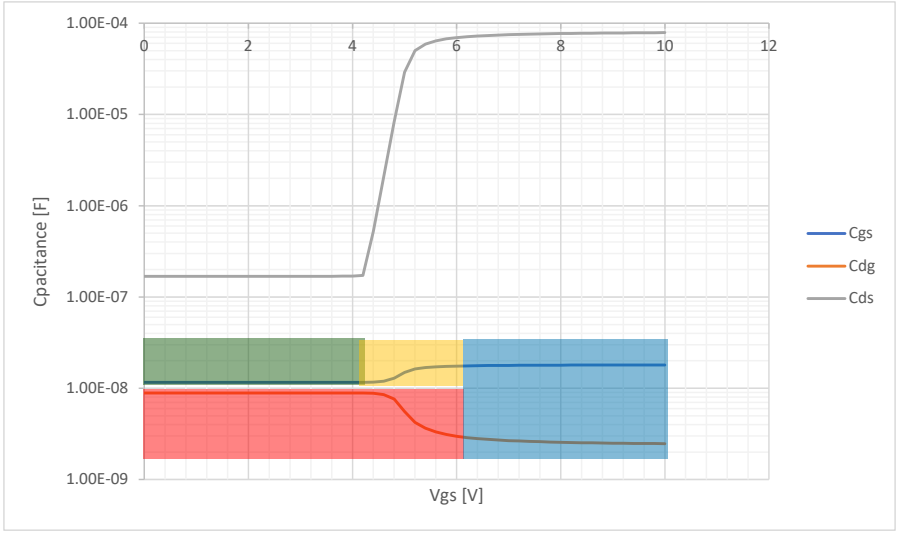
V_{GS}=f(Q_{gate}); I_D=58.2 A pulsed; parameter: V_{DD}

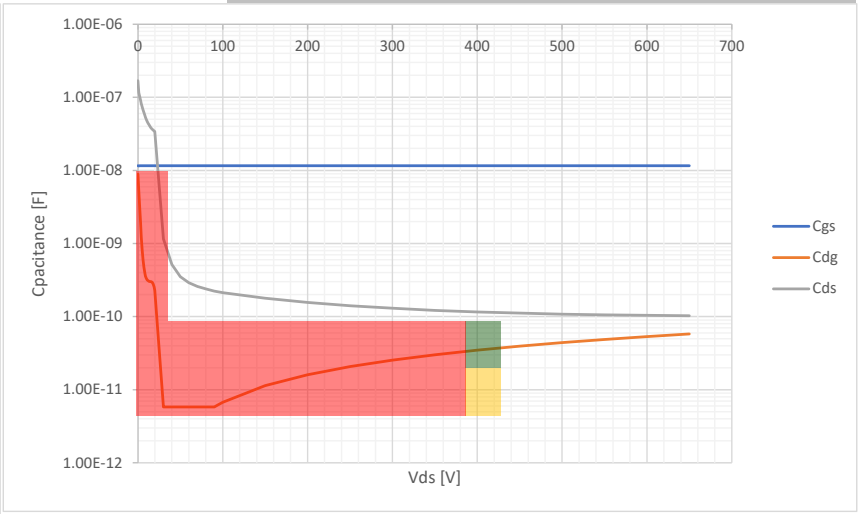
Infineon IPW65R022CFD7A
https://www.infineon.com/dgdl/Infineon-IPW65R022CFD7A-DataSheet-v02_01-EN.pdf?fileId=5546d46279cccfdb0179ccdff29c02d5

Simulated capacitors



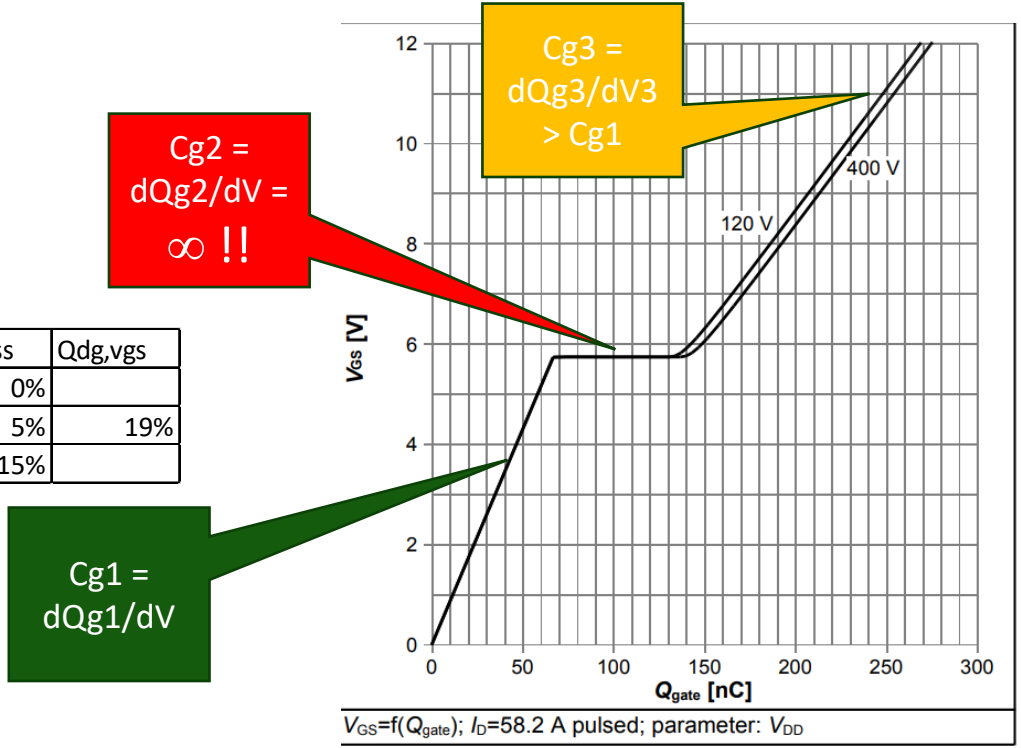
$Q_{gs,th}$ $Q_{gs,pl}$ Q_{gd} $Q_{gs,pl} \Rightarrow Q_{gs,max}$





Interpretation

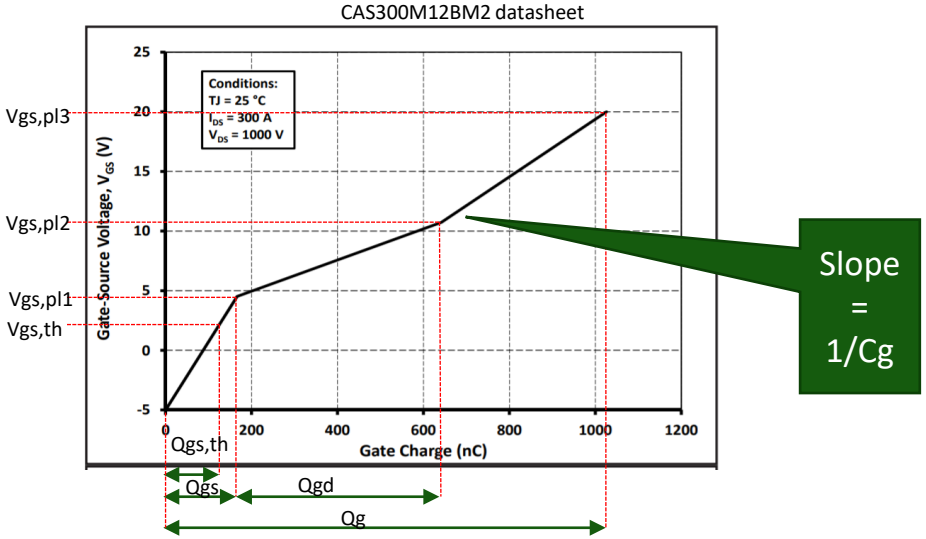
	Qgs	Qdg,rss	Qdg,vgs
Qgs,pl	28%	0%	
Qdg		5%	19%
Qg,pl - Qg, max	32%	15%	



Infineon IPW65R022CFD7A
https://www.infineon.com/dgdl/Infineon-IPW65R022CFD7A-DataSheet-v02_01-EN.pdf?fileId=5546d46279cccfdb0179ccdff29c02d5

Transistor charges define speed limits

- Current slew rate
  - $\frac{dI_d}{dt} = \frac{I_d . I_g}{Q_{GS} - Q_{GS,TH}}$
- Voltage slew rate
  - $\frac{dV_{ds}}{dt} = \frac{V_{BUS} . I_g}{Q_{GD}}$



Power transistor loss revisited

- **Gate loss** : $P_g = Q_g * V_g * f_{sw}$
- **C_{oss} loss** : $Pc_{oss} = C_{oss,loss} * V_{sw}^2 * f_{sw}$
- **R_{dson} loss** : $P_{rds} = R_{dson} * I_{out}^2$
- **Switching loss** :
  - $P_{sw} = V_{sw} * I_{out} * (t_r + t_f) * f_{sw}/2$
  - Area 3 + Area 5
- **Reverse recovery loss** :
  - $P_{rr} = (I_{out} * t_a + Q_{rr}) * V_{sw} * f_{sw}$
  - Area 1 + 2 + 4

Figure 13: Ideal current and voltage waveforms of a switching cell during MOSFET turn-on phase and diode turn-off phase

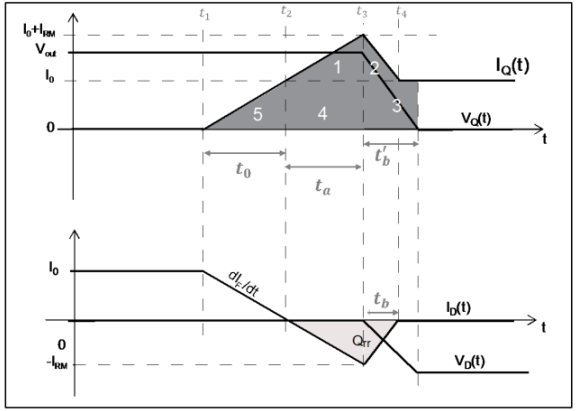
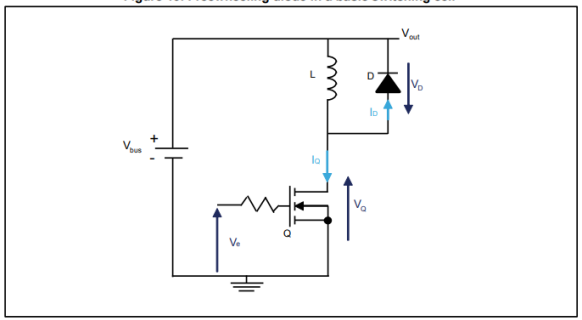


Figure 10: Freewheeling diode in a basic switching cell



Ref: ST AN5028 : Calculation of turn-off power losses generated by an ultrafast diode

Benchmarking GaN, Si & SiC

Based on commercial 1200V devices

	SiC	GaN	Si	Unit
Qg*Rdson	5…10	0.2 … 0.4	100…150	mOhm*uC
Coss*Rdson	5..12	5…12	120…340	mOhm*nF
Rise/falltimes	50	5	50	ns
Reverse recovery energy*Rdson	0.01	-	3	mOhm*mJ

Benchmarking SiC/GaN/Si

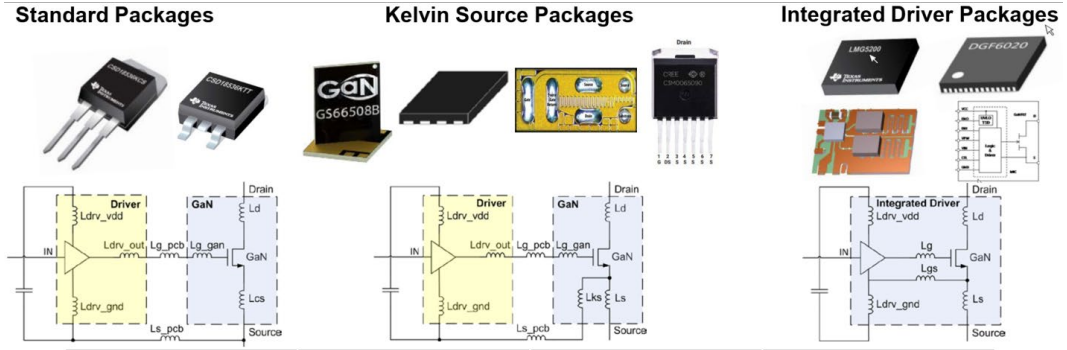
- **High power density**
  - SiC (SKM350MB120SCH15) : 19.5 Ohm*mm² (1200V)
  - GaN (VM40HB120D) : 125 Ohm * mm² (1200V)
  - GaN (GS66508B) : 3 Ohm*mm² (650V)
  - Si (APT28M120B2) : 244 Ohm*mm² (1200V)
- **SiC and GaN have no/little reverse recovery**
  - yielding lower switching losses
  - Lower current spikes during switching transitions => potentially better EMI
- **Higher temperature capability** for GaN and SiC
  - In practice, packages are limited to 200°C

Package limited driving speed

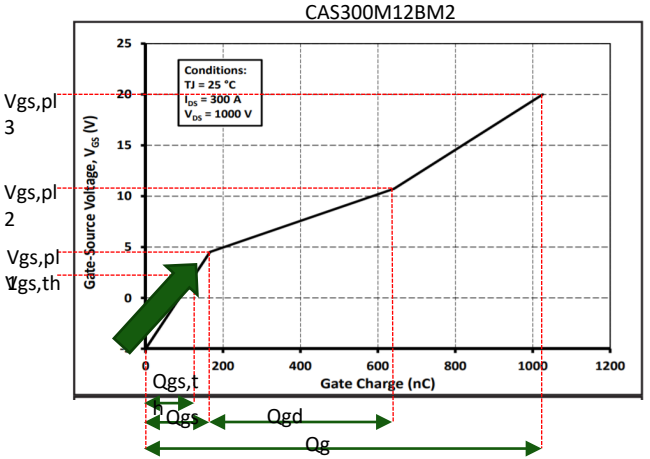
- Current slew rate limited by common source inductance

$$\frac{dI_d}{dt} = \frac{V_g - V_{gs,pl}}{L_{package}}$$

- L_{cs} = 5nH => P_{sw} + 60%



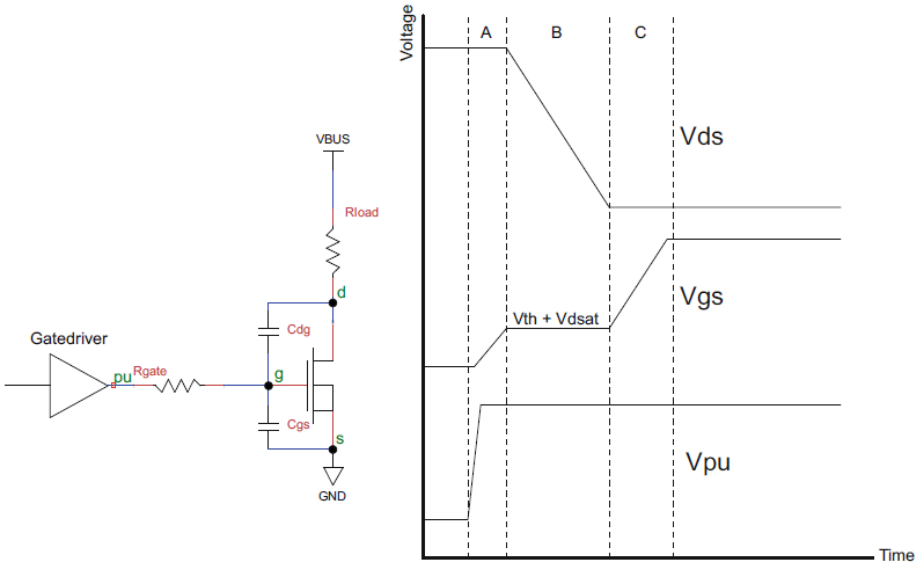
	Standard Power Package	Kelvin Source Power Package	Integrated Driver Power Package
Common Source	2nH -10nH	<1nH	<1nH
Gate Loop	5nH – 20nH	5nH – 20nH	1nH – 4nH



Ref : "Electrical and Thermal Packaging Challenges for GaN Devices", Paul Brohlin, Texas Instruments, PwrSOC 2016

Gate driving in practice

- **A** : precharge from 0 (or negative voltage) to Vth + Vdsat
  - Not useful -> keep as short as possible
  - Current switchover starts at Vth -> Vth+Vdsat
- **B** : defines dV_{ds}/dt. (may be absent in case of inductive loads, allowing ZVS)
- **C** : charge from Vth+Vdsat to full Vgs.
  - Keep as short as possible : reach steady state Rdson as fast as possible (Rdson losses)

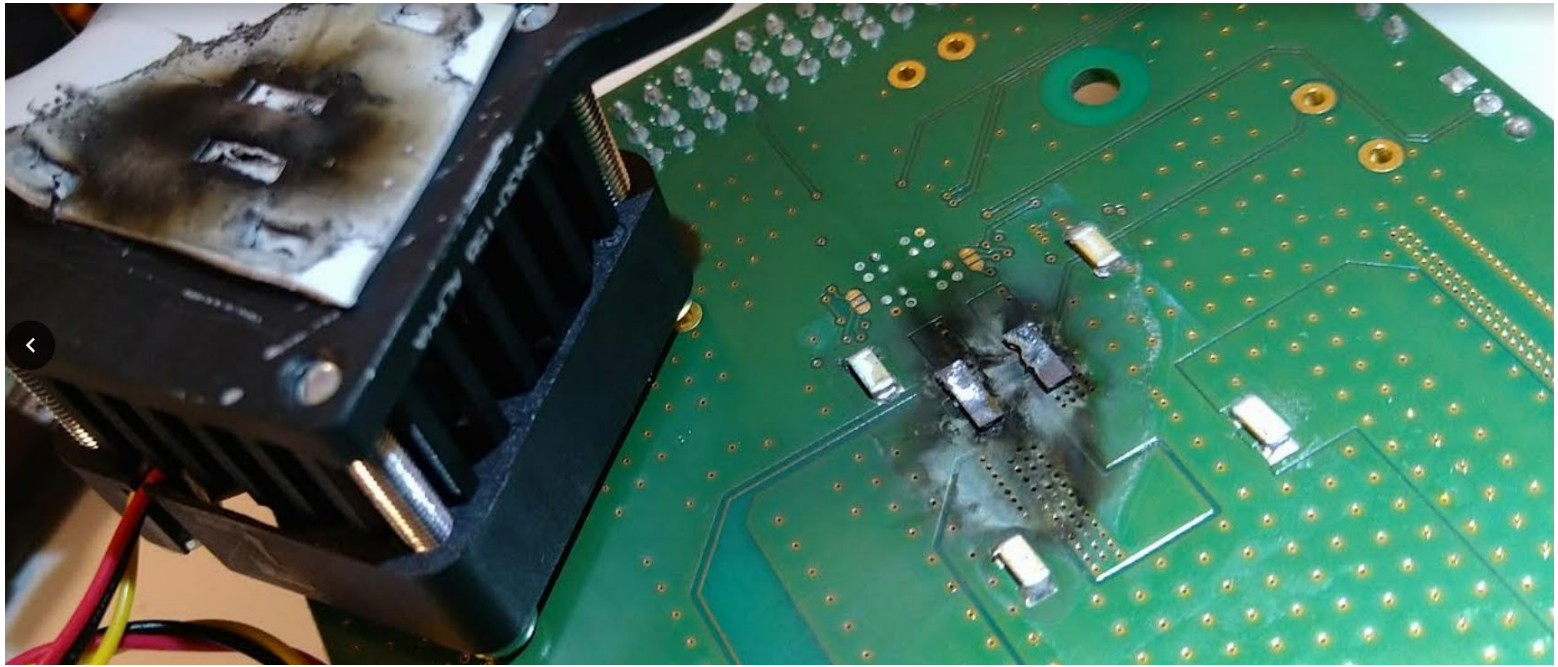


Why driving with a resistor?

- **Gate loss** : $P_g = Q_g * V_g * f_{sw}$
  - Dissipating in the gatedriver is costly (die area) or impossible (eg lack of cooling)
  - Rg keeps gate loss power outside the driver
- **Gate source parasitic inductance**
  - $e = L_{gs}\, di_{gate}/dt$
  - Either limit inductance (impossible for OTS power FETs)
  - Or dI/dt, by adding Rg
- **Imperfect Kelvin gate connections**
  - $e = L_s\, di_{source}/dt$
  - Slow down switching Vds at cost of power, but slower Ids change as well.

Challenges in GaN HEMT driving

- Magic Smoke will appear if you treat a GaN HEMT like a MOSFET.



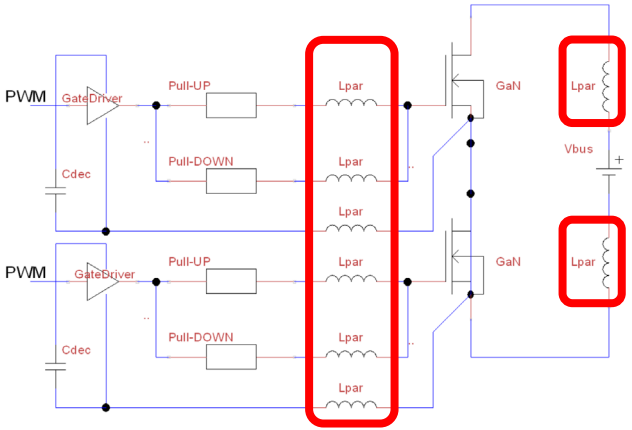
Challenges in GaN HEMT driving

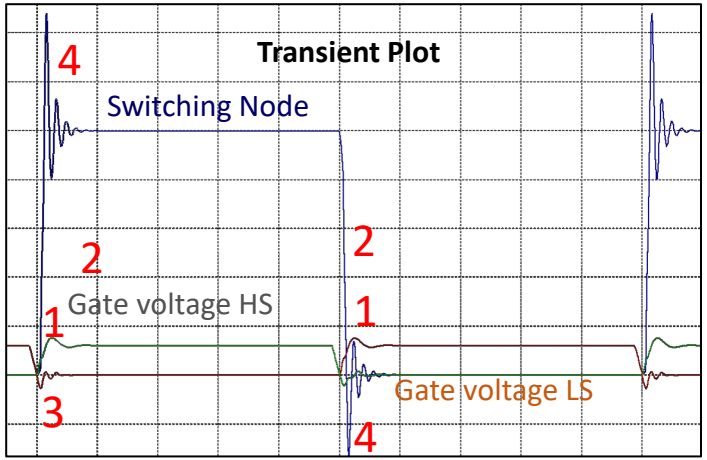
Potential	Issue	Solutions
Lower switching losses through faster turn-on/off times	high dV/dt will actuate all parasitic L/C Bus decoupling becomes critical	Low inductance packages ☺ (Switch slower ☹)
lower Pcoss (Lower Rdson * Coss)	None	
No reverse recovery losses	Considerable larger reverse conduction “diode” voltage compared to MOS during dead-time	Active dead-time control / dead-time tuning Gate sensing
Lower gate drive losses (Lower Rdson*Qg)	Low Cgs/Cdg combined with high dV/dt and low Vth can cause parasitic turn-on	Optimize gate loop inductance ☺ Switch negative (Switch slower ☹)
	Negative bridge voltage during dead-time can cause overcharging	Tight control of the gate turn-on voltage
Higher power density (lower Rdson*Area)	Heat needs to be evacuated efficiently	Low Rth packaging Trade-off thermal board layout with power routing :-/
Lower thermal mass	Limited short-circuit capability (<100ns!)	Fast active short-circuit protection

Challenges in GaN HEMT driving

On PCB level

- Gate-loop inductance
  - Over-voltage stress on the gate 1
  - Limits transient speed 2
  - Parasitic turn-on 3
- Supply inductance
  - Ringing on switching node 4
  - Limits transient speed 2

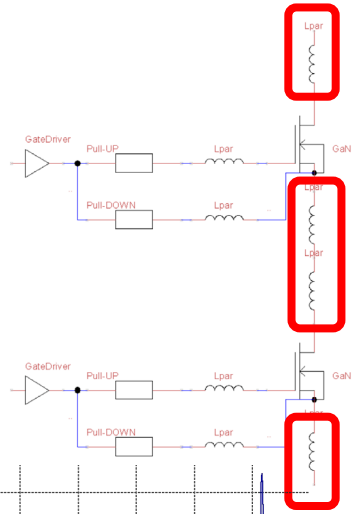


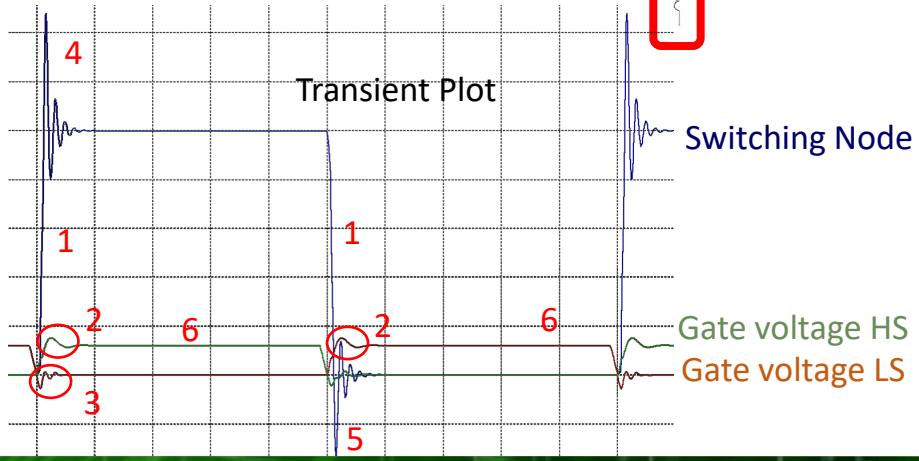


Challenges in GaN HEMT driving

On PCB level:

- Gate resistors
  - Regulates transient speed 1
  - Keeps dissipation outside driver
  - Dampens the gate LC 2
  - Prevents parasitic turn-on 3
- Drain-source inductance
  - Ringing on switching node 4
  - Negative voltage on driver 5
  - Over-charges bootstrap 6

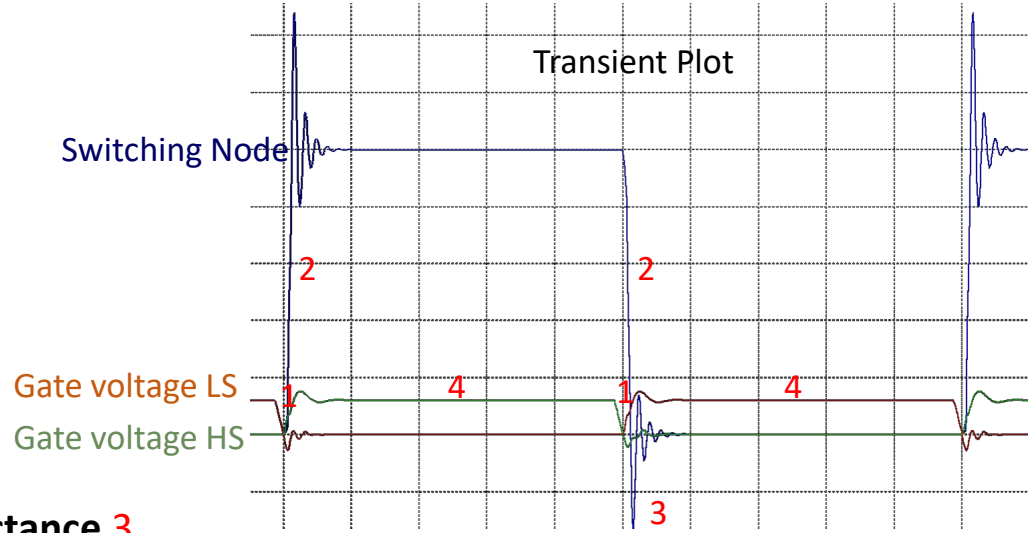




Challenges in GaN HEMT driving

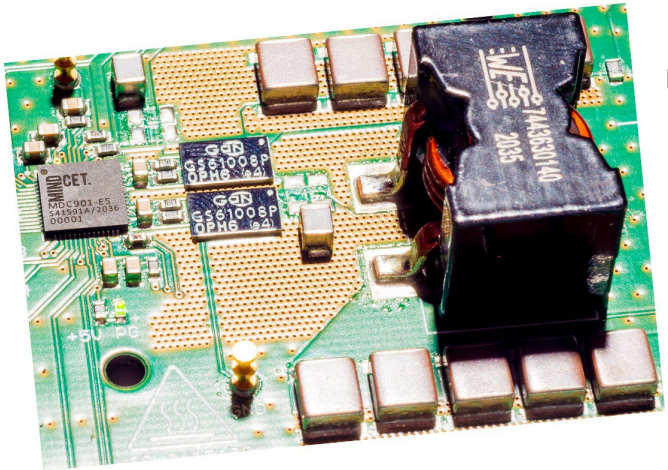
On Driver level

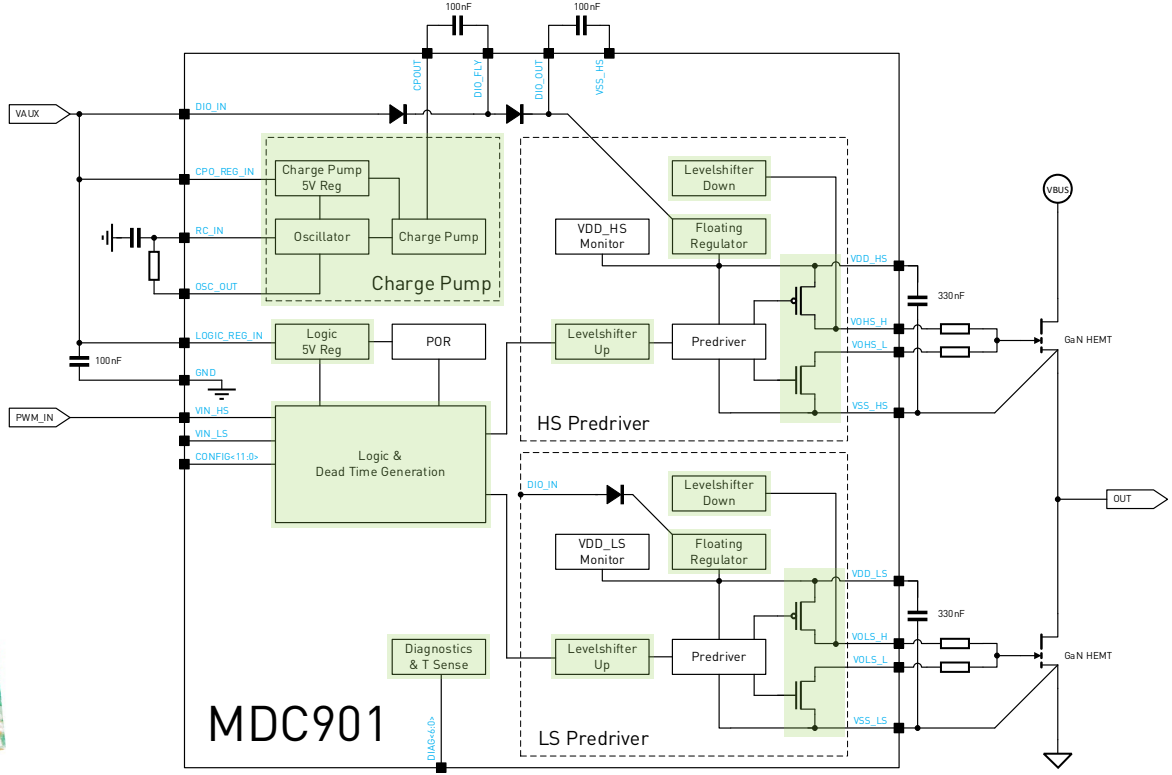
- **Dead-time control** 1
  - Cross currents in GaN
  - Recirculation loss
- **LS/HS delay-matching** 1
  - Cross currents in GaN
- **dV/dt** 3
  - False gate commutation
  - Driver failure
- **Negative Source voltage = GND inductance** 3
  - False gate commutation
  - Driver failure
  - Bootstrap over-charging -> Gate-stress and breakdown 4



Challenges in GaN HEMT driving

- **MDC901** : 200V High/Low side GaN predriver





Solutions in Predriver + GaN HEMT driving

Potential	Issue	Predriver solution
Lower switching losses through faster turn-on/off times	high dV/dt will actuate all parasitic L/C Bus decoupling becomes critical	**Levelshifters allowing large CMTI (100V/ns)**
lower Pcoss (Lower Rdson * Coss)	None	
No reverse recovery losses	Considerable larger reverse conduction “diode” voltage compared to MOS during dead-time	**Automatic and feedforward dead time generation with ns propagation delay matching**
Lower gate drive losses (Lower Rdson*Qg)	Low Cgs/Cdg combined with high dV/dt and low Vth can cause parasitic turn-on	**10-A peak source,17-A peak sink driver currents**
	Negative bridge voltage during dead-time can cause overcharging	**Down to -4V GaN source operation guaranteed**
Higher power density (lower Rdson*Area)	Heat needs to be evacuated efficiently	**Driver allows for -40 to 125°C ambient operation**
Lower thermal mass	Limited short-circuit capability (<100ns!)	Fast active short-circuit protection

Solutions in Predriver + GaN HEMT driving

- some OTS GaN gate drivers will provide bootstrap diodes, sometimes with a voltage clamp
- During dead time, OUT node will switch negative
- VCC-VOUT needs to be clamped to the gate driver to protect the GaN gate
- Floating supply principle
  - Regulator before UVLO/clamp
  - Whatever VCC-VOUT is, right voltage will appear at supply of the gate driver
  - Reliable operation of the GaN HEMT is guaranteed
- Overcharging can also happen at the LS!

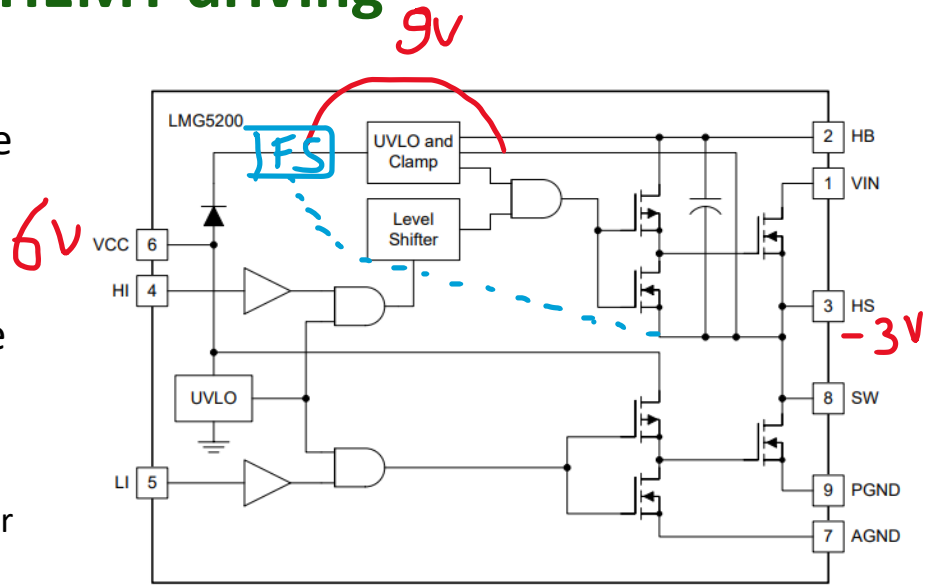


Figure 10. Functional Block Diagram

Ref : LMG5200 datasheet https://www.ti.com/lit/gpn/lmg5200

Solutions in Predriver + GaN HEMT driving

- **Non-overlap / deadtime** : why ?
  - Don't we want to avoid quadrant 3 operation ?
  - We do, but…
    - When $I_{inductor} > 0$: Coss will be discharged by the inductor while sweeping low.
    - When Iinductor < 0 : Coss will be charged by the inductor while sweeping high
    - => depending on the load conditions, applying a certain amount of deadtime will increase the efficiency through ZVS!
- **Programmability**
  - HS and LS gate drive train have certain propagation delay (may be matched on chip)
  - Propagation delay will vary as function of supply voltage temperature and between parts/
  - Programmable deadtime is a must for maximal efficiency

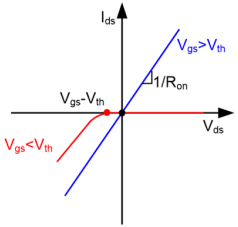


Figure 4. Simplified Behavior of GaN in the First and Third Quadrant

Ref:
http://www.ti.com/lit/SNOAA36

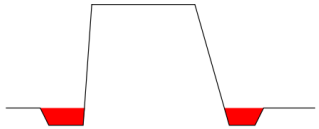


Figure 1. Idealized Buck Switch Node Waveform. The Red Area is the Dead Time Loss.

Ref:
http://www.ti.com/lit/SNOAA36

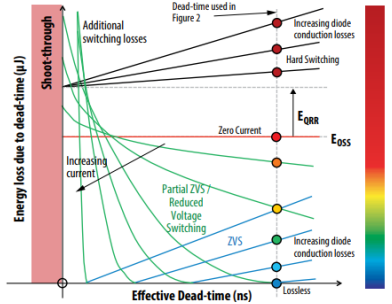
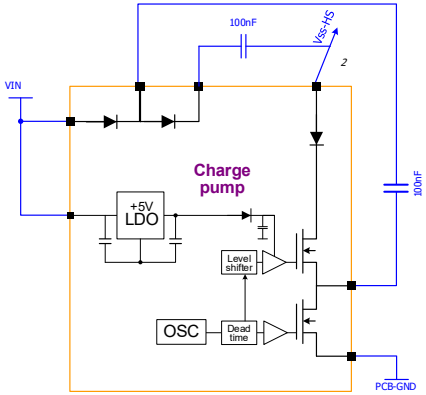


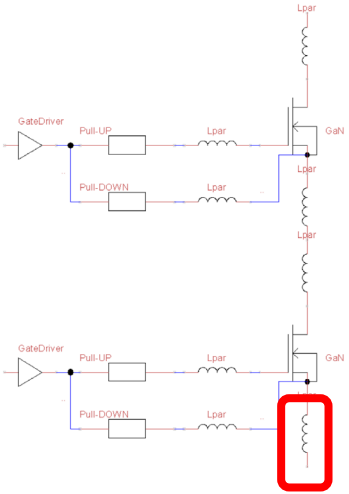
Figure 3: Idealized dead-time related loss per cycle for different load currents versus dead-time (Red to blue coloring represents high loss to no loss)

https://epc-co.com/epc/Portals/0/epc/documents/papers/Dead-Time%20Optimization%20for%20Maximum%20Efficiency.pdf

Solutions in Predriver + GaN HEMT driving

- **100% dutycycle?**
  - High-side driving applications and motor control application can work at very long on-times
  - Charge cannot be maintained by bootstrap diode + Cap alone
  - Chargepump is needed => will provide trickle charge to allow bootstrap to maintain its level.
- **Integrated bootstrap diodes**
  - Both HS and LS
  - Very fast, low trr
  - Provides symmetry in drive strength
  - Source inductance can bounce the power ground up/down with several volts. Bootstrapping allows for isolation from the input supply
  - In MDC901 HS and LS are interchangeable!





Solutions in Predriver + GaN HEMT driving

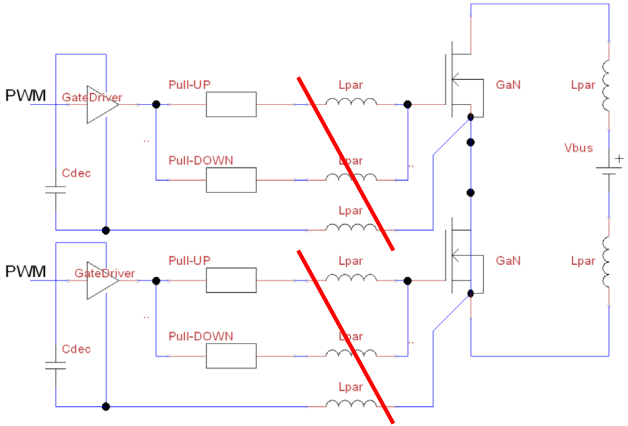
- **Safety : protect your precious GaN device**
  - UVLO to monitor the floating supply levels => avoid insufficient gate drive
    - Tristate in case of UVLO active
  - Temperature sensing : internal die temperature is sensed and can be used for overtemperature protection
  - Gate voltage monitoring: gate voltage is levelshifted back to the ground domain: offers startup control
    - Or advanced automatic dead time generation
  - Error detection in case HS / LS don’t switch

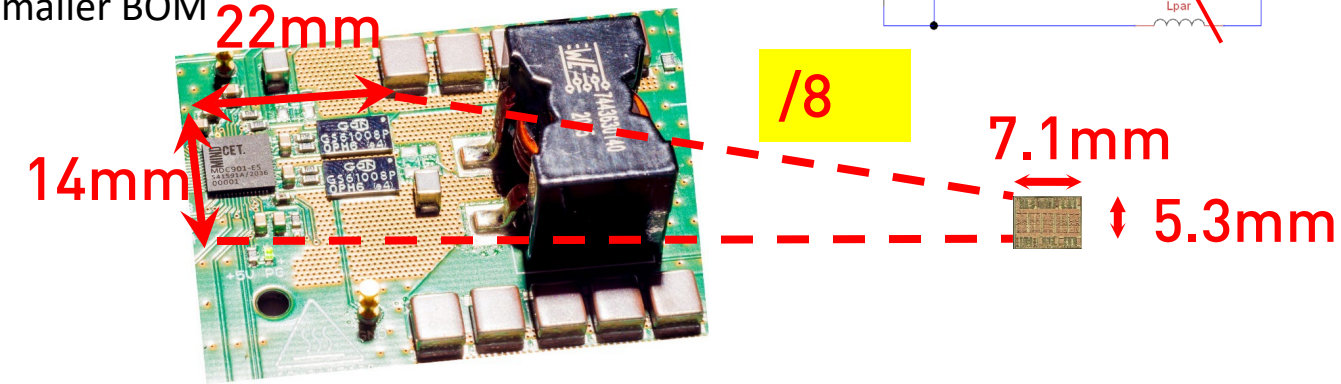
Solutions in Predriver + GaN HEMT driving

- **Hostile environment robustness**
  - **dV/dt immunity**
    - Aka Common mode transient immunity
    - Levelshifter needs to work reliably within the expected slew rates of GaN : 100V/ns
    - How : depends on the (lack of) isolation
      - Symmetry
      - Parasitic extraction
      - Hard lessons…
  - **Negative swing immunity**
    - Parasitic inductance + 3th quadrant operation will let your driver swing below ground
    - The levelshifter needs to stay operational down to -5V
    - The levelshifter needs to keep its state preferably down to -10V

The route to monolithic integration : 4 reasons

- Reliability: minimize the gate voltage overshoot
- Killing the gate loop inductance, getting the GaN up to speed $\frac{dI_d}{dt} = \frac{V_g - V_{gs,pl}}{L_{package}}$
- Higher power density
- smaller BOM



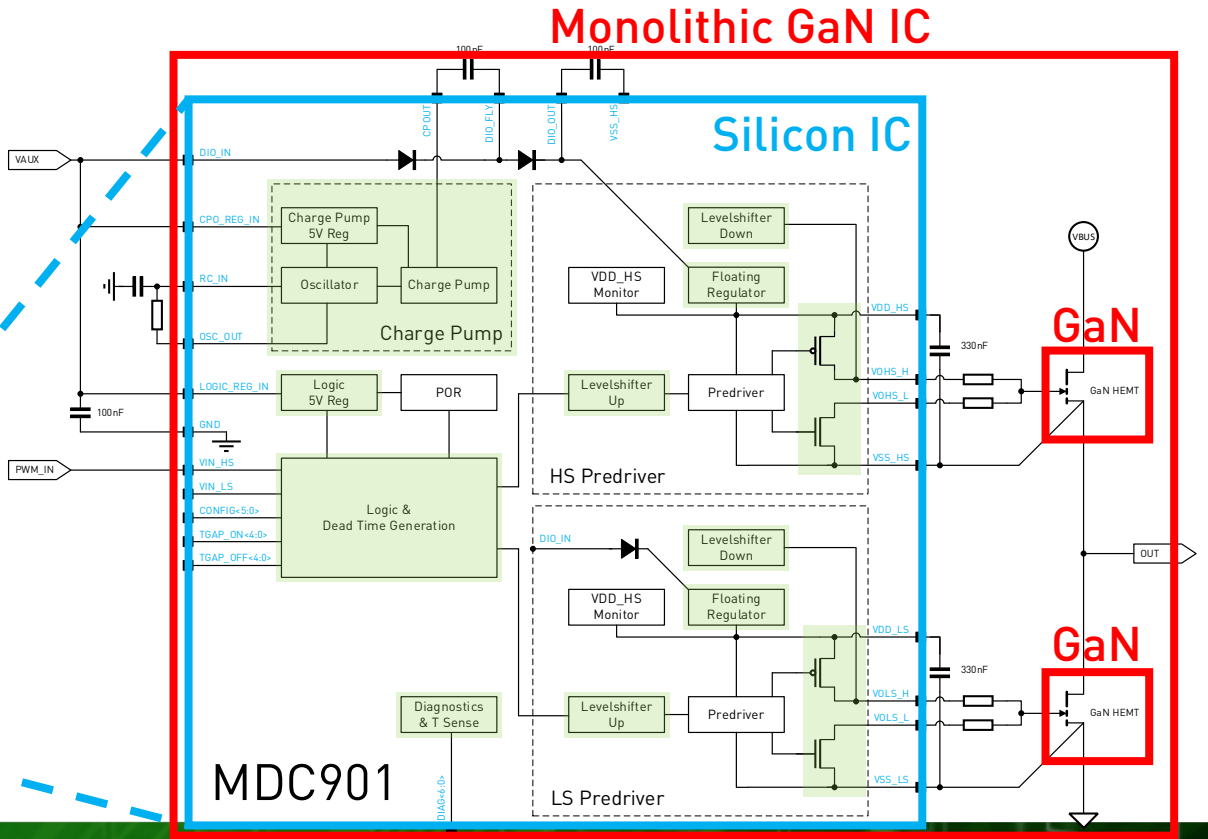


The route to monolithic integration

Co-integrate

Gate driver and

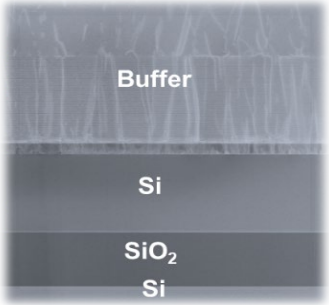
GaN power stage



The Ultimate Solution: Monolithic GaN ICs

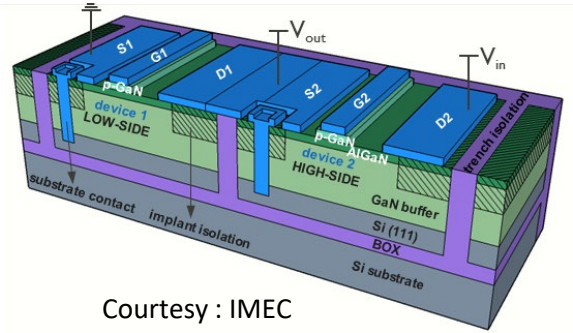
- SOI wafer as base for GaN HEMTs

TEM cross-section of GaN/AlGaN superlattice-based buffer on SOI substrate.



Courtesy : IMEC

- DTI to electrically insulate HEMTs from each other



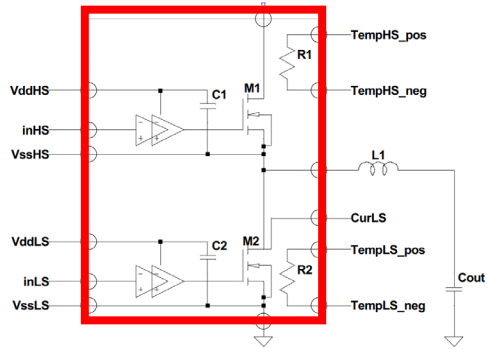
Courtesy : IMEC

Schematic cross-section of GaN-on-SOI structure, featuring buried oxide, oxide filled deep trench, local substrate contact and p-GaN HEMT devices.

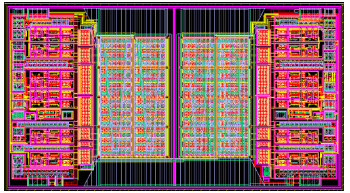
Point-of-Load GaN IC Implementations

- Monolithic Half-Bridges for PoL DCDC
- 200V / 10A RMS
- HS & LS Gate-Drive integrated
- HS & LS decoupling / BS cap integrated
- <10ns propagation delay
- ns turn-on/off
- LS current sensing
- Temperature sensing

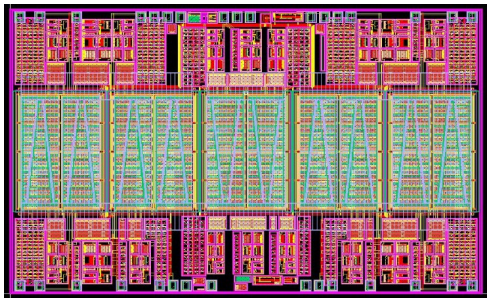
No concerns about the gate-driver



32 + 32 mΩ (19.5mm²)

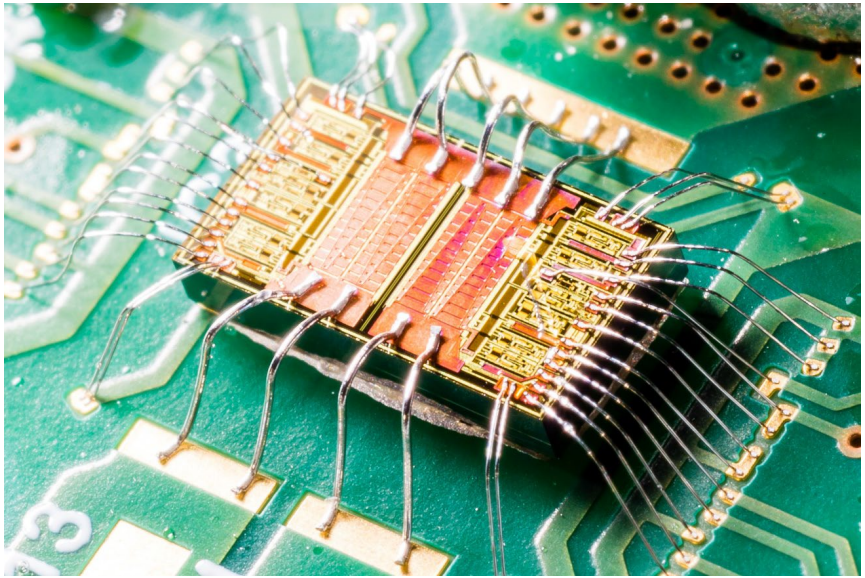


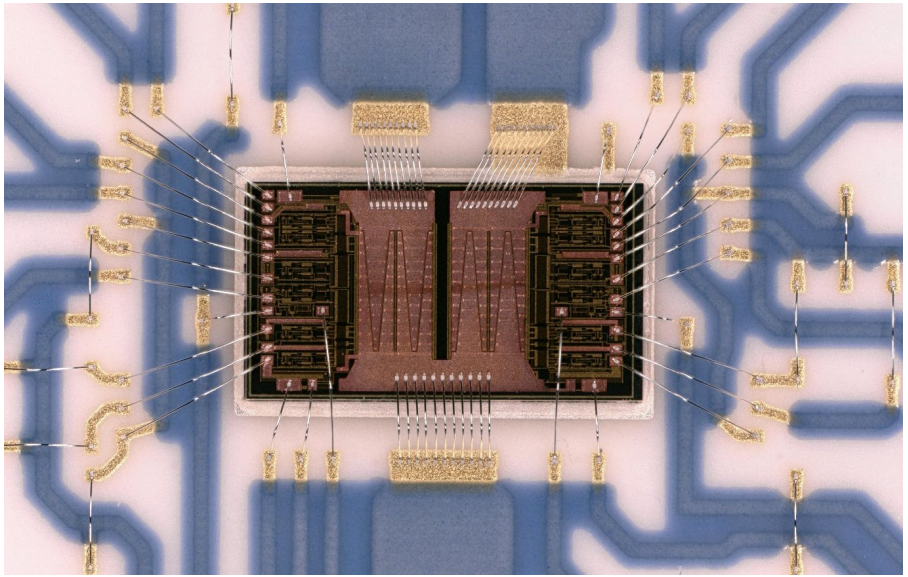
32 + 8 mΩ (38.5mm²)



Point-of-Load GaN IC Implementations

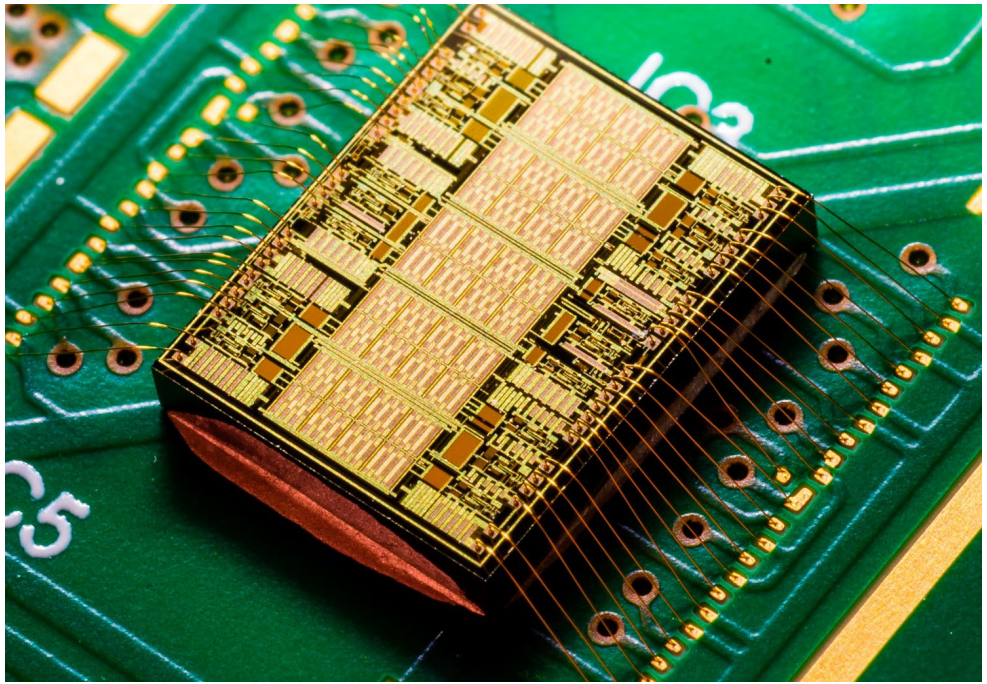
- First Iteration: The Assembly symmetrical version Chip-on-Board: FR4 and AluOx





Point-of-Load GaN IC Implementations

- First Iteration: The Assembly asymmetrical version
- Relative contribution of BW
  - Rdson
  - Inductance ?
- Industrial applications:
  - BGA type

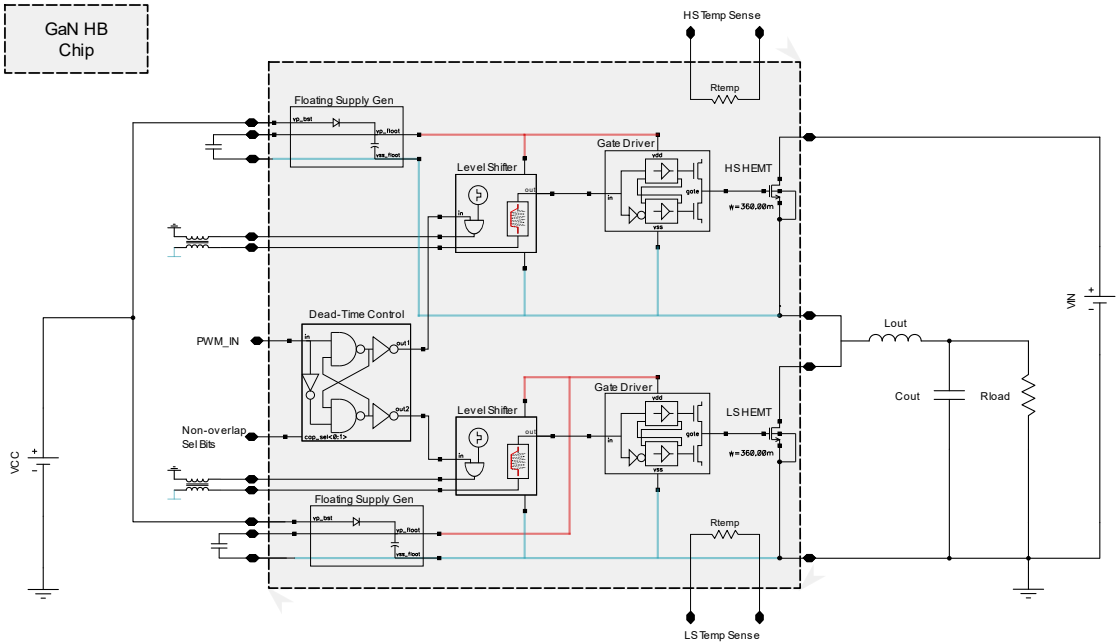


Point-of-Load GaN IC Implementations

Second Iteration

- Monolithic Half-Bridge for PoL DCDC
- 200V / 10A RMS
- HS & LS Gate-Drive integrated
- HS & LS decoupling / BS cap integrated
- Isolated level-shifter integrated
- HS & LS Floating Supplies for gate-drive
- Dead-time control integrated
- Temperature sensing
- No more gate loop inductance
  - Direct drive of the GaN power device
  - Ideal connectivity of kelvin source
- Tight control of the gate drive levels
  - On chip preregulator

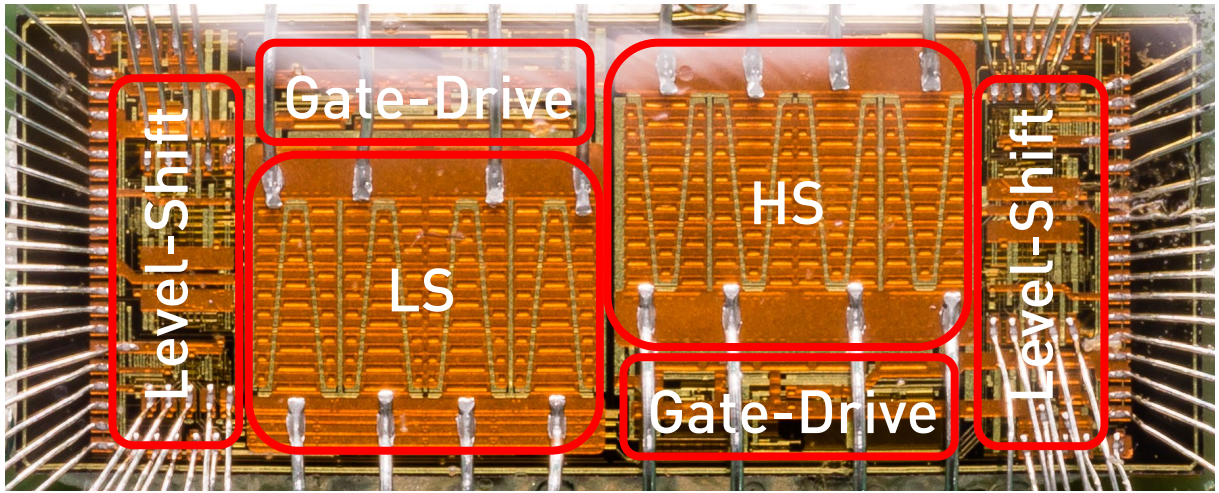
No concerns about the gate-driver!



Point-of-Load GaN IC Implementations

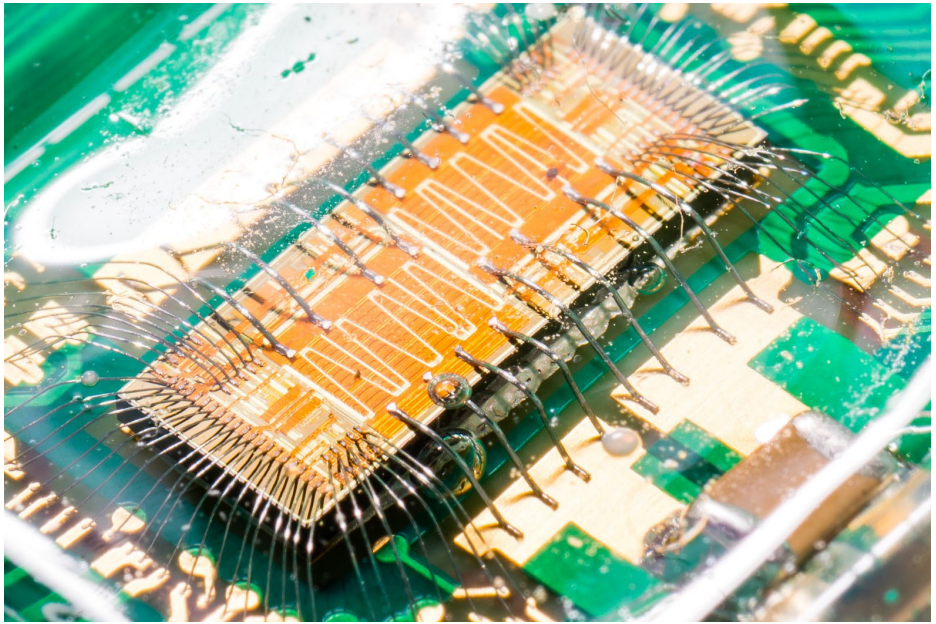
Second Iteration: The Real Thing

- 9.3 x 3.8mm²
- GaNIC4S ESA Project



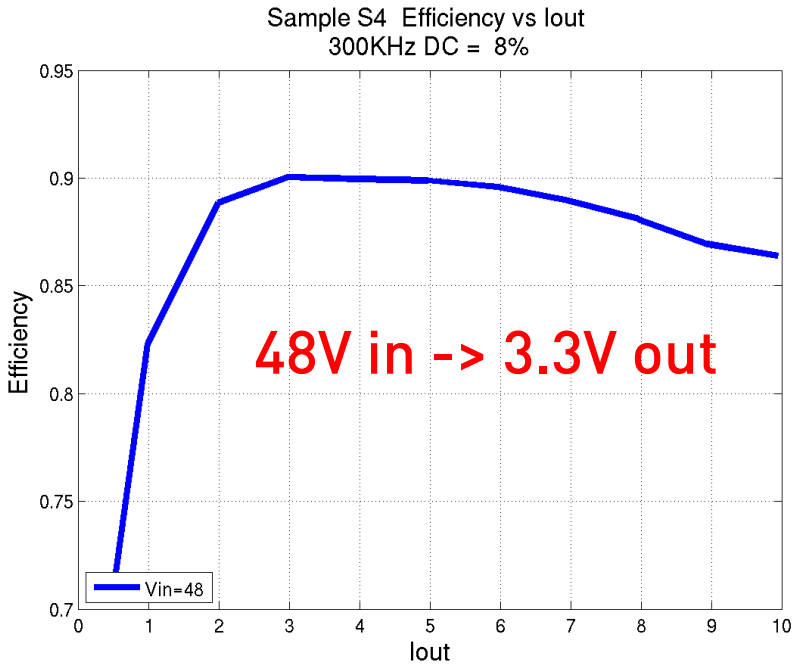
Point-of-Load GaN IC Implementations

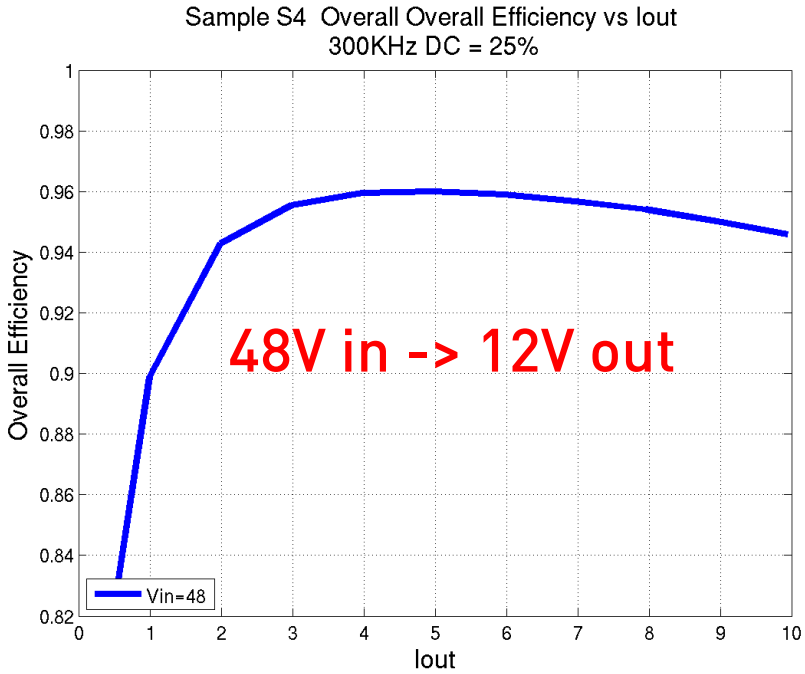
- Chip-on-Board: FR4
- 125um Bondwires for Power
- 50um Bondwires for signals & test pads



GaN IC Measurements

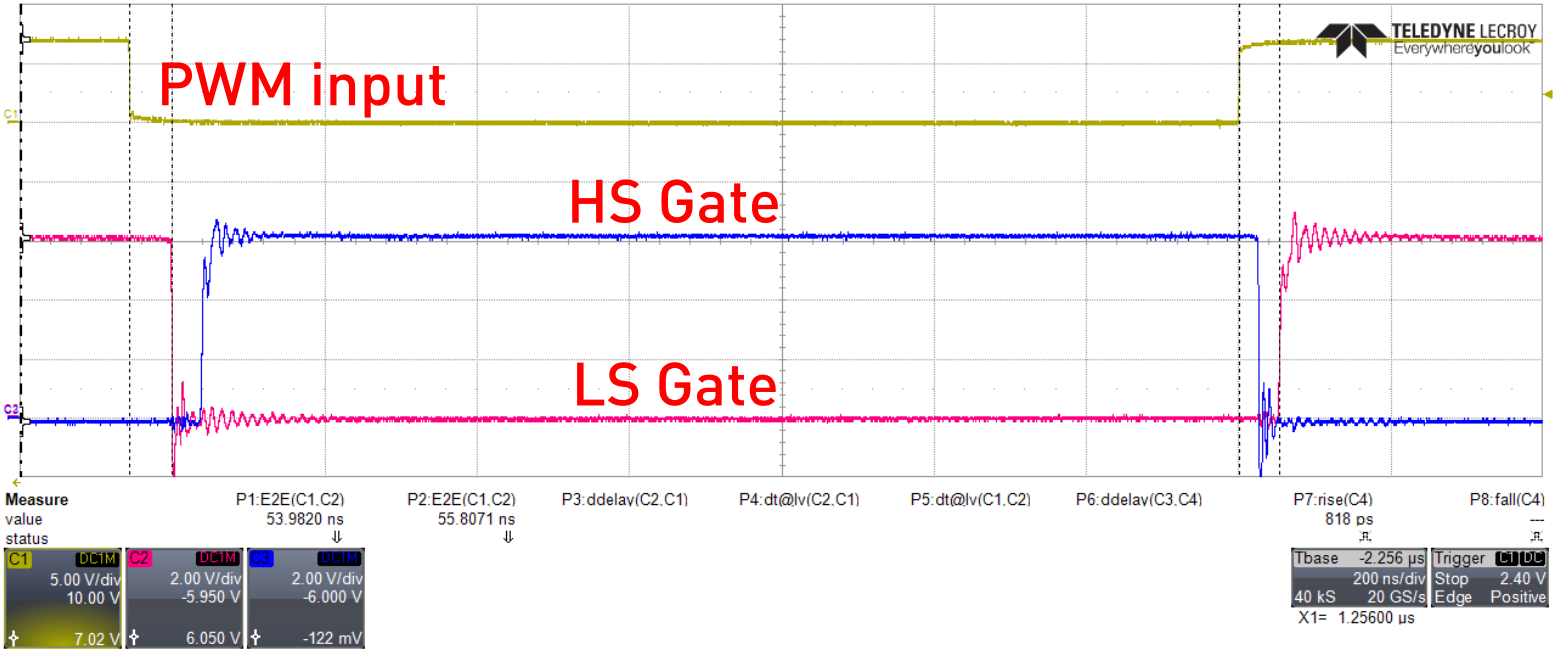
- Second Iteration Efficiency (22uH inductance)





GaN IC Measurements

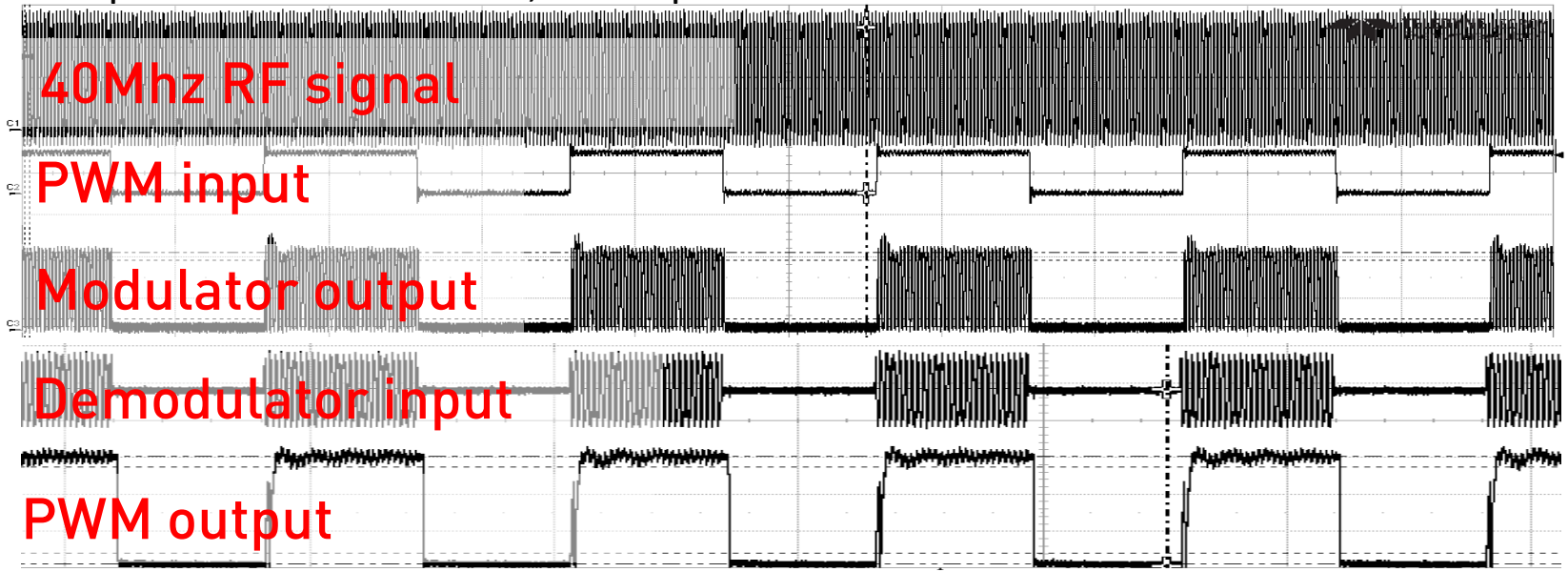
- On-chip dead-time generation



GaN IC Measurements

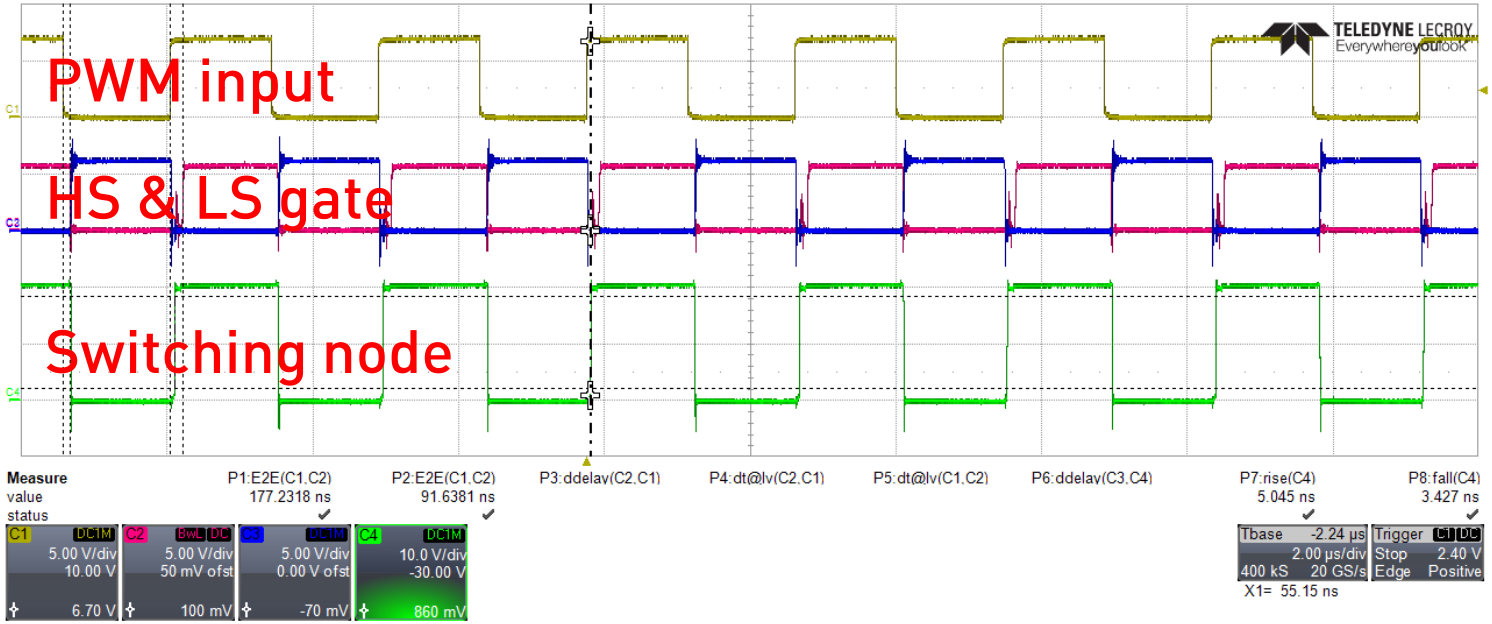
- Second Iteration Signals

- On-chip Isolated Level-Shifter, off-chip transformer



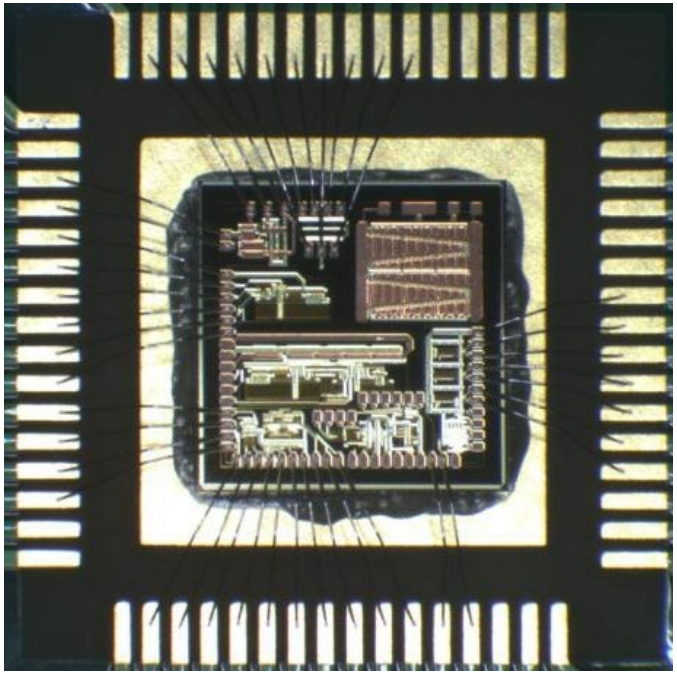
GaN IC Measurements

- Switching Buck Converter



Future Work

- Measure prototype resistive type level-shifters (no galvanic isolation, higher speed)
- Development of over-current / de-saturation protection
- Development of current sensing
- Development of closed-loop control system
- Thermal aspects
- VBUS decoupling



Conclusions

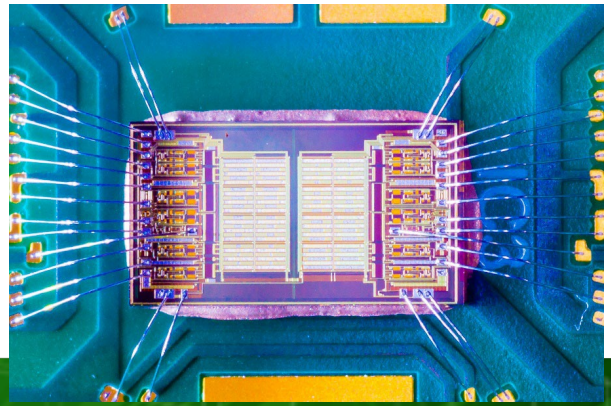
- GaN HEMTs are not inexpensive components, thus to maximize GaN benefits -> Get Your Gate DRIVE(R) Right!
- Monolithic GaN IC enables the true benefits of GaN
  - transient speed
  - low losses
  - Reliability
  - Power density
- The future of GaN is monolithic power stages and integrated gate-drive + level-shifters

Acknowledgments

- Project SloGaN “System Level Optimization of GaN-based power devices” funded by Agenschap Innoveren & Ondernemen (VLAIO) and ICON

https://www.imec-int.com/en/what-we-offer/research-portfolio/slogan

- Project GANIC4S “Monolithic integration of GaN gate driver and power transistor switching functions” under ESA Contract No. 4000128515/19/NL/FE



Ed Session

Pushing the Boundaries of Wide-Bandgap Power Conversion : a Journey Towards Monolithic Integration

Jef Thoné , MinDCet

The global climate change - urging for lower carbon emissions - is thrusting the current wave of electrification. The hunt for lost Joules in electrical energy generation, storage and conversion is more important than ever.

In each of these steps, power stages, inductors and capacitors play a key role, transferring power with minimal losses. In the last decade, traditional MOSFET and IGBT power stages are increasingly replaced by GaN and SiC switches, as they present higher power density and lower losses for similar operating conditions. Unfortunately – driving GaN or SiC is not as forgiving as driving a MOSET or IGBT, and offers new challenges to reach return-on-investment.

This tutorial treats the challenges and solutions towards maximized efficiency when driving wide-bandgap based power circuits – as well as a vision on the roadmap….

Jef Thoné received his Master of Engineering degree in Electronics at the Karel de Grote University, Antwerp, Belgium in 2002. From 2002 to 2006 he worked at Melexis Belgium as analog designer and project manager, on automotive sensor interface CMOS ASICs.
From 2006 to 2011 he worked towards his Ph.D. at ESAT-MICAS, KU Leuven, on telemetry for wireless capsule endoscopy.
In 2011 he and Dr. Mike Wens founded the company MinDCet, a Power IC design house based in Belgium. In his role of CTO, he lead the design of numerous high-voltage, high current and wide bandgap integrated circuits. He is co-holder of 2 granted patents on measurement systems for inductor and capacitor losses.