micas
KU LEUVEN

# MICAS Highlights 2023

# Welcome to the MICAS Highlights 2023

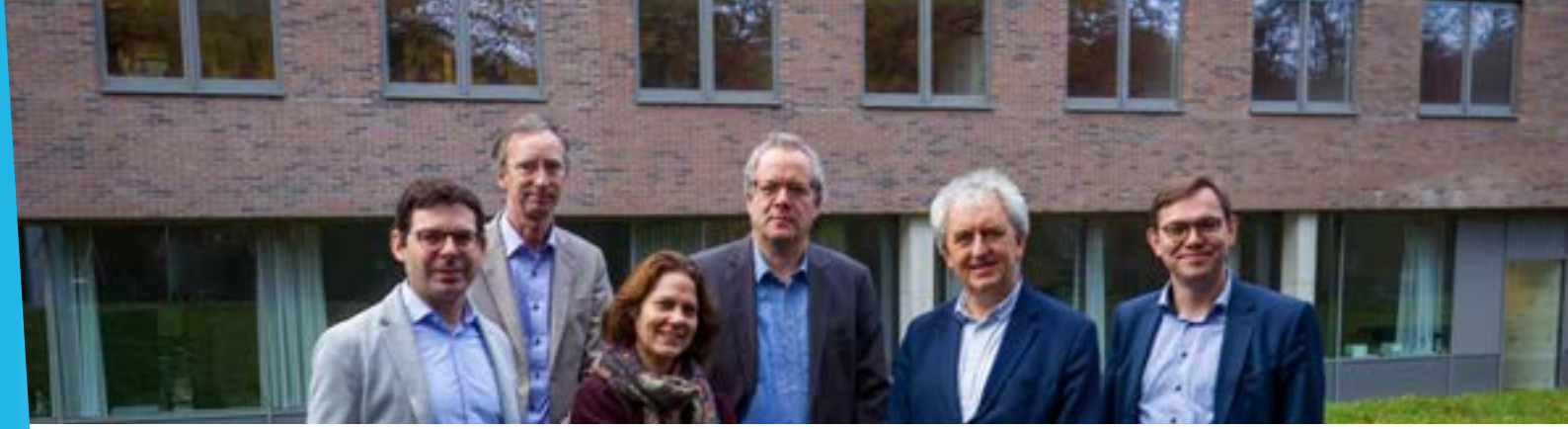
a booklet that shines a spotlight on the past year's most remarkable achievements and advancements within our research division...

At MICAS, we are guided by a mission encapsulating three fundamental pillars: Research, Educate, and Inspire. While scanning through the Highlights, you will experience our commitment to each of these pillars. Moreover, it will become clear that we are not only performing blue-sky research, but that we are also linking our research activities to the current and future societal challenges and opportunities.

2023 was the breakthrough year of AI tools like ChatGPT. But these tools consume a lot of energy and other resources. A widespread use of AI will only be possible if the algorithms can be executed in a much more efficient way. At MICAS, the ambitious new ERC project BINGO has been initiated to tackle exactly that challenge. This project underscores our dedication to pioneering research that will shape the future landscape of AI systems and their applications.

Moreover, we have not only one, but two ERC projects running at MICAS, which is a great testament of the excellence of our research and our academic staff. The second ERC project, called AnalogCreate, focuses on the autonomous creation of analog integrated circuits based on self-learning of design expertise.

Another fantastic achievement in 2023 was the honor of receiving the Bell Labs Prize for our groundbreaking work on terahertz imaging. This technology, bridging the gap between optical cameras and radar systems, holds the key to revolutionizing vision systems, for example in the field of autonomous vehicles. It shows how we are pushing the boundaries of what is possible, guided by our tagline, "the next circuits for a better life".



Recognizing the pressing need to address the talent shortage in the chip design ecosystem, we are excited to announce a new course series dedicated to chip development. By nurturing the skills and knowledge of the next generation of chip designers, we aim to contribute significantly to the growth and sustainability of this critical industry.

While Moore's Law keeps on going, we are proud to share that MICAS continues to secure access to the most advanced semiconductor technologies, mostly through collaboration projects with semiconductor companies and foundries. This is crucial for maintaining the industrial relevance of our work, ensuring that we remain at the forefront of innovation.

Finally, it is our pleasure to announce that MICAS will organize the largest European chip design conference ESSERC (formerly named ESSCIRC/ESSDERC) in the historical city of Bruges, Belgium, on September 9-12, 2024. This conference brings together the brightest chip designers and device engineers from academia and industry to discuss the most recent research achievements, blended with enlightening keynote talks and an extensive tutorial program. Being the 50th edition, we are working towards an excellent technical program offering combined with plenty of networking opportunities. Don't miss this ESSERC 2024 event in Bruges!

As you read through the MICAS Highlights 2023, we hope you get a flavor of the passion, dedication, and ingenuity that characterizes our team. This is a good moment to express our heartfelt gratitude, to our researchers, and to our support staff. And last but not least, we want to thank all our partners, as our collaboration has been the cornerstone of our success. Together, let us continue to push the boundaries of chip design, inspired by the belief that our work today shapes the circuits that will define a better life tomorrow.

Wim Dehaene
On behalf of the MICAS staff
January 2024

# Our mission

The three aspects of our mission are closely intertwined

## RESEARCH

Through our research, we define and answer fundamental challenges in the field of chip design and generate breakthroughs that enable new solutions based on microelectronics, both in academia and in industry.

We push research to its technological limits, starting from visionary ideas, to developing them into silicon proven concepts that are picked up by the industry.

## EDUCATE

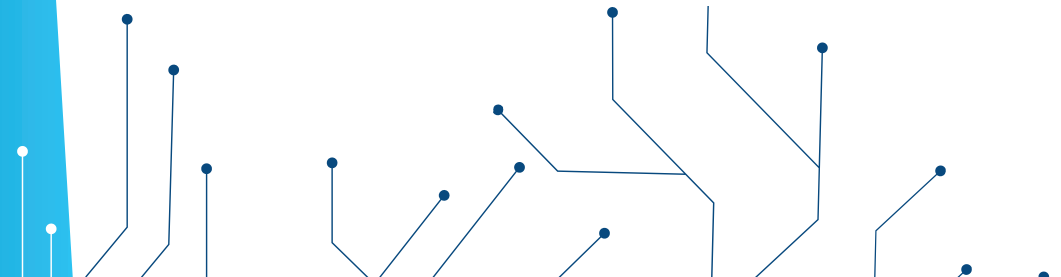
Rooted in our excellent research, we educate students to become leaders in electrical engineering and offer them the opportunity to further develop into PhDs.

Investing in our talented master and PhD students, by training them, by supervising them closely, sets them up to push the state of the art in circuit design.

## INSPIRE

We want to make society aware of the role and importance of microelectronics and enthuse people to participate in this exciting field.

Building the next generation of circuits and sensors for a social, comfortable, healthy, safer and sustainable life.



# Research

Through our research, we aim at defining and answering fundamental challenges in the field of chip design and generate breakthroughs that enable new solutions based on microelectronics.

**MICAS pursues a wide range of fundamental to applied research across nine research domains, which cover different aspects of integrated circuit design:**


- Analog and power management circuits 8-11
- Mixed-signal circuits and data converters 12-15
- RF, mm-wave and THz circuits 16-19
- Wireline and optical circuits 20-23
- Computer-aided hardware design and test 24-27
- Ultra-low-power digital SoCs and memories 28-31
- Hardware-efficient AI and ML 32-35
- Biomedical circuits and sensing interfaces 36-39
- Quantum and cryogenic circuits 40-43

## Research approach

The MICAS research agenda spans a very wide range: from fundamental to applied research, from conceptual explorations to chip prototype realizations. As such, a research project at MICAS typically goes through the following sequence of steps:

- Investigation of an innovative concept towards an implementable architecture;
- Design and fabrication of a demonstrator chip to validate the research results;
- Characterization of the chip in our in-house measurement labs;
- Analysis of the results as a starting point for a next design cycle.

This sequence is then repeated such that the initial concept can gradually mature into research results that can be transferred to industry and society. The many projects in the MICAS research pipeline are funded through various channels: from internal KU Leuven and basic science funding, over Flemish and European funding, often in collaboration with industry, to bilateral industrial funding. The Intellectual Property arrangement is tailored towards the specific type of collaboration, meeting the exclusivity requirements of our partners without blocking our own academic freedom and research roadmap. In addition to our research on chip innovations, we also investigate and develop computer tools and methodologies to more efficiently design and test chips, and we work on innovative algorithms and modeling methods to address problems not (yet) covered by commercial tools. More information can be found on the Research Domain pages.

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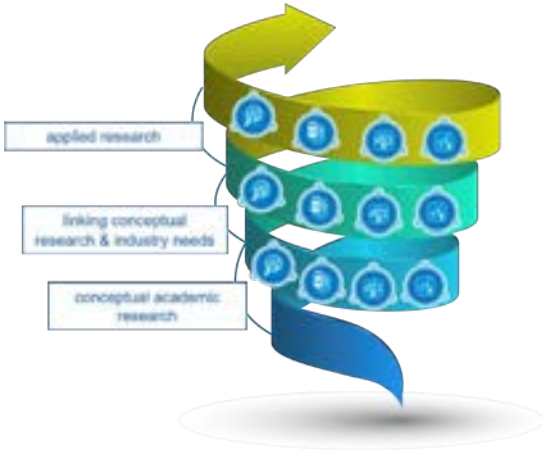


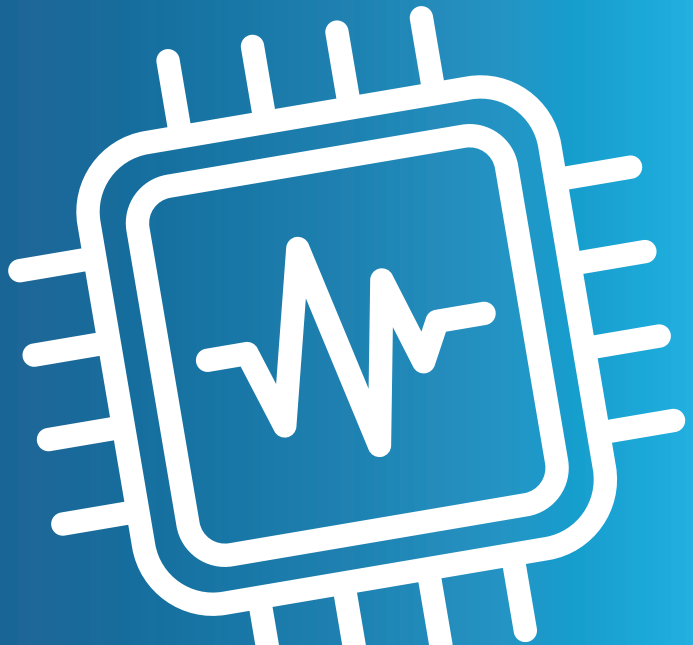

Learn more about some of our projects on our website.

# Analog and power management circuits

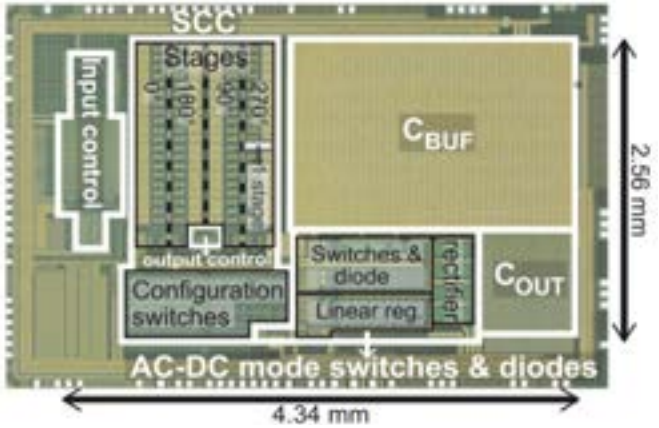
## “Analog circuits are vital components in our highly digitized society.”

Analog circuits remain vital components in our highly digitized society. Analog circuits span various challenges and applications, ranging from analog front ends, amplifiers, filters, etc. Scaled CMOS technologies, with their reduced supply voltage and intrinsic gain, challenge such building blocks fundamentally.

Additionally, more advanced power management circuits are emerging as power efficiency is critical to increasing battery life and enabling ever more powerful applications. The trend towards higher voltages, higher power densities, higher conversion ratios, and a higher integration level remains relevant. MICAS is a strong player in all these domains. We focus on innovative approaches and on the use of standard CMOS and more innovative integration technologies.

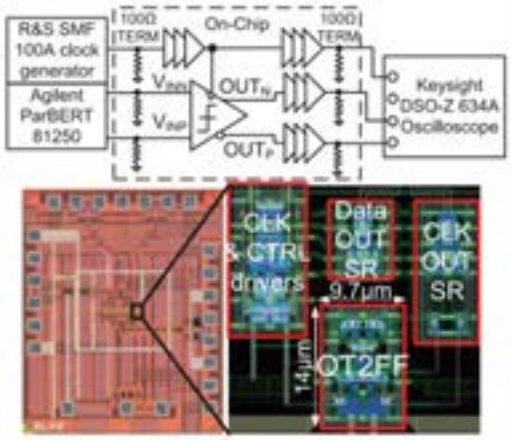


# 2023 highlights on analog and power management circuits




## A fully integrated 230 VRMS-to-12 VDC AC-DC converter

We have fully integrated a 230 VRMS-to-12 VDC AC-DC converter in 180 nm high-voltage CMOS SOI. The AC-DC converter includes a multi-ratio switched-capacitor DC-DC converter. The reconfiguration is realized by parallelizing stages using low-voltage switches. Internally generated DC nodes are connected, resulting in low losses. The input control includes a resettable capacitive divider with >250× less losses than a resistive divider. The measured power density is 9 mW/mm² at 53.1 % efficiency, advancing the power density of fully integrated state-of-the-art AC-DC converters by >5000×. This work was presented at the 2023 VLSI Symposium.




## High-speed comparators with reduced delay slope

Comparators are the most critical component in many systems, ranging from wireline receivers to high-speed and high-resolution ADCs. One of the defining parameters is the delay slope, i.e. the rate at which the comparator delay increases with decreasing input signals. This potentially leads to metastability resulting in significant performance degradations regarding BER in the mentioned applications. We have presented several state-of-the-art comparators in the last years, culminating in our 10 GHz quadruple-tail comparator with double feedforward paths. The prototype comparator in 28 nm CMOS achieves 26.4 ps delay at a 1 mV input and -5.8 ps/decade delay slope. It achieves the shortest delay and the smallest delay slope of any recently published high-speed comparator. Furthermore, it shows a flat delay and noise across input common mode from 0.4 V to 0.8 V. This work was presented at ESSCIRC 2023.

### Driving large ultrasound transducer arrays for haptic feedback

Haptic feedback is attractive for all kinds of man-machine interfaces and gaming. It is a touch sensation generated in the human skin by a modulated and focused ultrasound (US) beam. To generate such a beam, large US transducers in TFT technology are needed. Driving these arrays is a circuit design challenge taken up by MICAS. In 2023, we published two driver arrays dealing with all the challenging circuits aspects in different TFT technologies. Power efficiency enhancement with advanced charge recycling and novel synchronization techniques are the most striking examples. The required synchronization accuracy goes beyond what is achievable in TFT technology. This led to the development of a hybrid/TFT architecture with a current based interfacing technique to exploit the capabilities of both technologies. The design of hybrid Si/TFT circuits is a topic we will further work on in our future research. Stay tuned! This work was published in the IEEE Journal of Solid-State Circuits.


# Contact

Analog and power management circuits

**Prof. F. Tavernier**
filip.tavernier@kuleuven.be

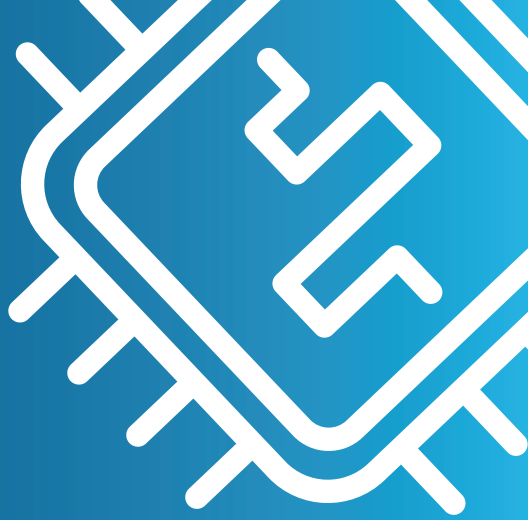
**Prof. M. Steyaert**
michiel.steyaert@kuleuven.be

"Analog and power management circuits remain at the core of our research even as technology scales and our world becomes more digital."

## Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

# Mixed-signal circuits and data converters

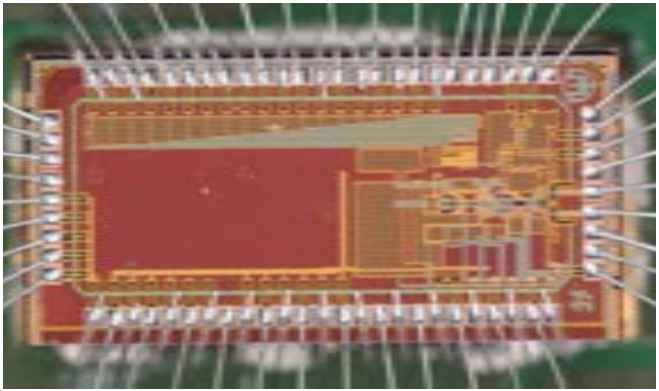


"Data converters interfacing the analog and digital realms are among the most critical components of most modern electronic applications."

Data converters interfacing the analog and digital signal realms remain among the most critical components of many modern electronic applications. The need to faithfully preserve the signal across domains continues to pressure data converters to deliver a higher bandwidth and linearity while reducing the power consumption.

Exciting new architectures and circuits are continuously being introduced that push data converters towards ever higher performances. MICAS has always been a renowned contributor in this domain. This trend continues as we work on various innovative architectures and circuit building blocks, focusing on low latency, high input bandwidth and increased energy efficiency for edge and sensing applications.

# 2023 highlights on mixed-signal circuits and data converters

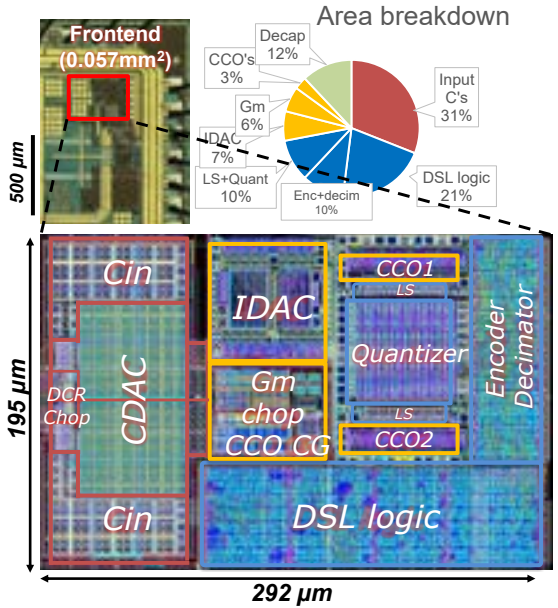


### Open-loop residue amplifiers in low-latency precision ADCs

Combining low latency with high precision is challenging as many ADC architectures realizing such high precision result in a significant delay between input and output. A pipelined converter with a limited number of stages (2 to 3) is promising in this regard, as it combines both a low latency, thanks to the limited number of stages, with a high resolution, enabled by the pipelining. However, a pipelined converter typically suffers from high power consumption in the closed-loop residue amplifiers. We have proposed the use of open-loop residue amplifiers for such applications, significantly reducing the overall power consumption.

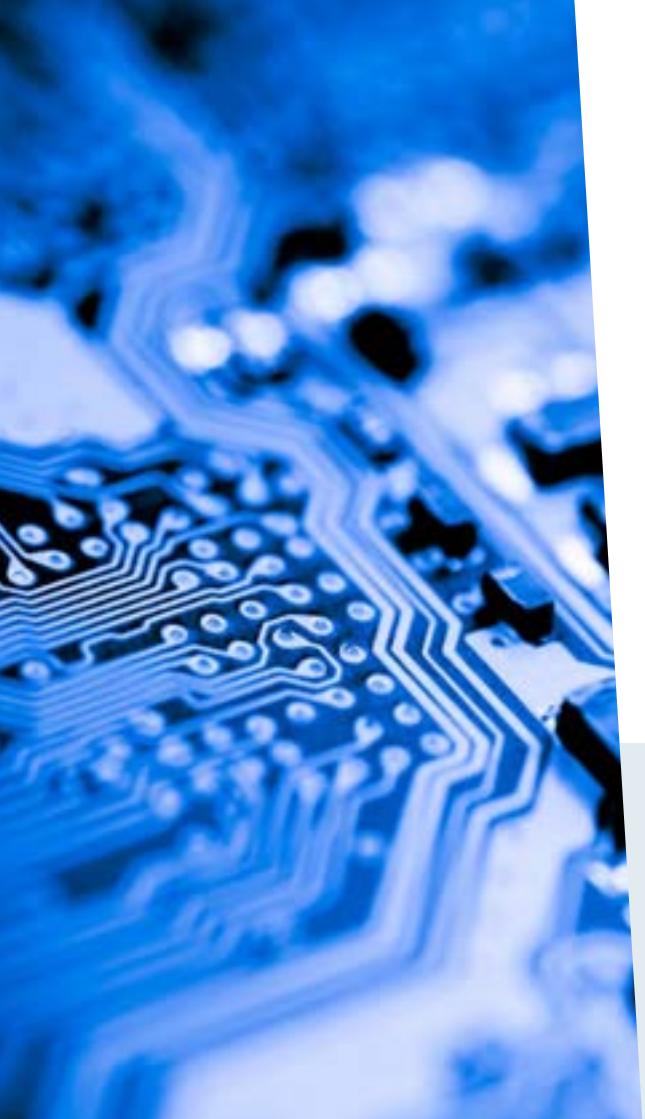
### Neuromorphic, event-driven level-crossing ADC with high power efficiency

Level-crossing analog-to-digital converters are neuromorphic, event-driven data converters that are suited for resource-constrained applications where intelligent sensing must be provided with tight energy and area budgets, such as in edge devices or biomedical implants. For time-sparse signals such as ECGs, neural action potentials, etc., these converters can result in significant data bandwidth reduction as well as save up to two orders of magnitude in chip area and system energy consumption compared to conventional ADCs. Their event-driven nature makes them ideal to generate spiking signals as inputs to spiking neural networks for tasks such as input signal classification. The level-crossing ADC architecture developed at MICAS has been improved further using fully adaptive resolution and clocking, further reducing the power while enabling multi-channel readout. In addition, we have shown that information metrics such as the Bayesian or (corrected) Akaike criteria can be used to tune the ADC's parameters to maximize the SNN classification accuracy. This work received international recognition as we won the 2023 Analog Devices Student Design Contest.




### Time-encoding VCO-based ADCs for ultra-low chip area and process scalability

Traditional voltage-mode ADCs lack scalability in advanced CMOS technologies. Due to their highly digital nature, time-encoding ADCs, on the other hand, offer an ultra-low chip area with good process scalability, while being on par with respect to power and resolution performances. The leading MICAS expertise in this field has been expanded further by developing a novel delay cell to implement a highly linear controlled ring oscillator. In addition, the performance feasibility of multiplexed incremental time-based sensors-to-digital $\Delta\Sigma$ readout has been demonstrated for the readout of neural signals; this work has been presented at the BioCAS 2023 conference.



# Contact

## Mixed-signal circuits and data converters

**Prof. G. Gielen**
georges.gielen@kuleuven.be

**Prof. F. Tavernier**
filip.tavernier@kuleuven.be

"Seamlessly bridging the analog-digital divide for a broad range of applications is at the forefront of our research."

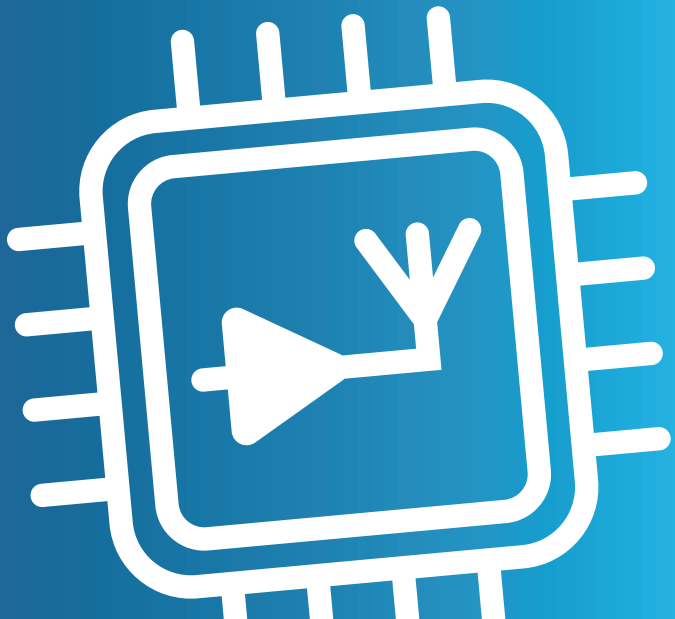
### Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

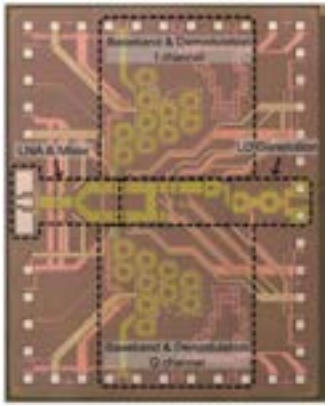
# RF, mm-wave and THz circuits

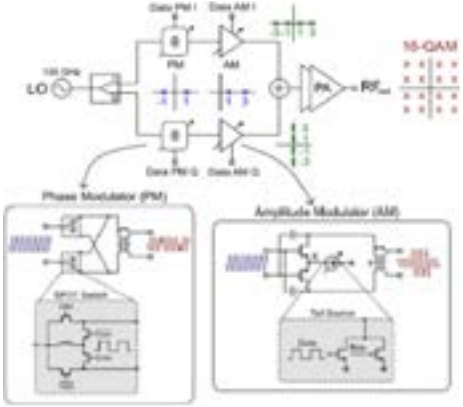
"MICAS has a long tradition in the broad field of RF circuits."

MICAS has a long tradition in the field of RF circuits in general. Whether it is for cellular 5G communication, unlicensed applications, radar, sensing, imaging or future 6G communication, the research in this field is continuing with a wide range of topics. As operating frequencies and -more importantly- bandwidths go up, novel architectures and circuit techniques are needed. Furthermore, the research on RF, mm-wave and THz circuits is also diversifying with respect to semiconductor technologies. Whereas a strong focus on standard CMOS has been the mantra of MICAS in the past, today a wide range of technologies, such as GaN, GaAs, InP, FDSOI and FinFET are being used in our research projects for future communication, ranging and sensing applications. This allows us to focus on the best technology for each specific application.



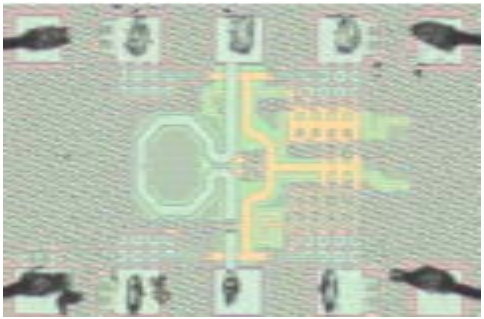
# 2023 highlights on RF, mm-wave and THz circuits





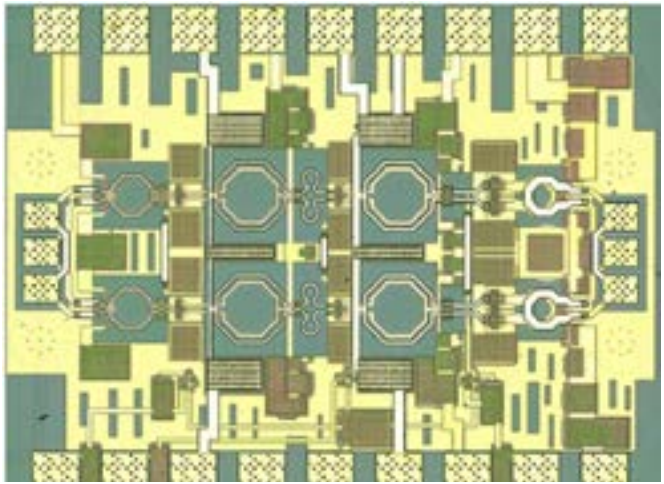

**135GHz direct-digital 16QAM modulation TX and RX chipset in 28nm CMOS**

As modulation bandwidths increase, it is becoming increasingly difficult to rely on classical TX and RX topologies. In this research, the approach of a Direct-Digital modulation was investigated. Based on a polar modulation architecture, consisting of a separate amplitude modulator and phase modulator, and this in combination with an I- and Q-signal branch, a 16-QAM constellation can be synthesized using simple NRZ signaling. This approach was implemented in 28nm CMOS, leading to a full TX and RX operating at 135GHz. With this chipset, we were able to achieve record data rates of up to 32Gbps over a wireless and a dielectric channel. The results have been published in the Journal of Solid-State Circuits 2023.



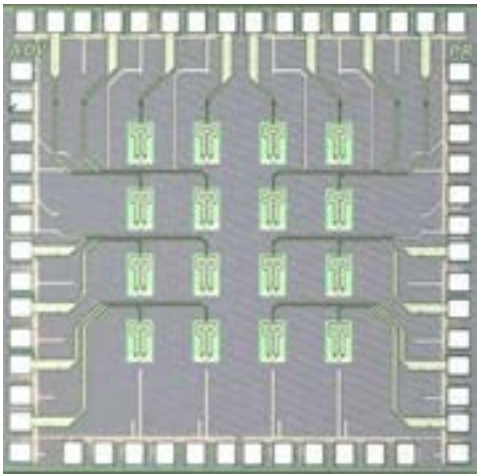
**Transformer-based mm-wave isolator in 22nm FD-SOI**

In 2023, we published the results of our research on transformer-based isolators. The circuit was implemented in 22nm FD-SOI and operates in the promising 36-40GHz frequency band. Being able to implement isolators in silicon allows to avoid bulky off-chip components and enables a further integration level, much needed for future beamforming systems. This research was in collaboration with iCana in Leuven and was published at the 2023 European Microwave Conference.



### InP D-band power amplifiers and THz oscillators

In collaboration with imec, various 6G communication circuits have been developed and measured in InP. To explore the limits of the technology, a 1THz oscillator was successfully designed and measured. In our measurement lab, the oscillation at 965GHz could clearly be observed. This work was presented at BCICTS2023. Furthermore, a D-band PA was implemented in the same 250nm InP technology and presented at RFIC2023. The clever biasing technique, needed to keep those bipolars in Class AB operation, received recognition as this paper was awarded as one of the Best Student Papers at the conference.



### A 4x4 THz image sensor in 28nm CMOS

Linear circuit operation is limited by fmax, the maximum frequency for gain and oscillations. But non-linear techniques can work above fmax. MICAS has been investigating injection locking as a way to develop very sensitive detectors above fmax in CMOS. This was presented at ISSCC2021, where a 600GHz detector with record low noise was presented. In 2023, we presented the follow-up work, also at ISSCC: a 4x4 THz image sensor, demonstrating that these self-oscillating pixels can also work in an array. On top of that, this innovative work received international recognition as we won the 2023 Bell Labs Prize.

# Contact

RF, mm-wave and THz circuits

**Prof. P. Reynaert**
patrick.reynaert@kuleuven.be

**Prof. M. Steyaert**
michiel.steyaert@kuleuven.be

"As operating frequencies and bandwidths go up, novel architectures and circuit techniques are needed."

## Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

# Wireline and optical circuits

"Answering the never-ending need for energy efficiency, higher speeds, and lower latency."

The research on wireline and optical circuits at MICAS is pushed by the never-ending need for energy efficiency, higher speeds, and lower latency. But at the same time, MICAS also explores innovative communication concepts such as full-silicon optical solutions enabling 1310/1550 nm communication and polymer microwave fibers (PMF).

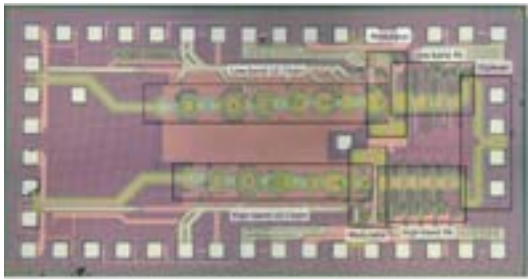
Optical interaction is highly challenging in silicon. The high doping concentrations and low supply voltages of CMOS result in small and slow responses of photodiodes. Moreover, 1310/1550 nm light is not absorbed due to the high bandgap. However, the trend towards higher integration levels can also be seen in this challenging domain thanks to innovative circuit techniques combined with novel conversion mechanisms between the optical and electrical domains. MICAS has been a trendsetter in this domain for many years.

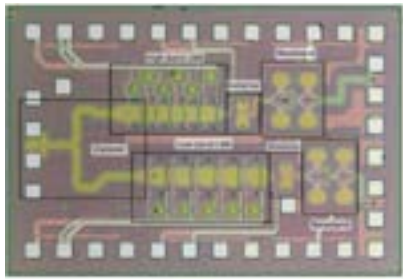
Also, concerning polymer microwave fibers, MICAS stays in the leading position by pushing the data rate and distance boundaries. Not only is the research investigating silicon integrated front ends for PMF, but also couplers, duplexers, and fibers are being investigated to obtain the optimal solution for a wide range of connectivity applications.

# 2023 highlights on wireline and optical circuits

### Demonstration of >100Gbps Polymer Microwave Fiber links using 28nm CMOS

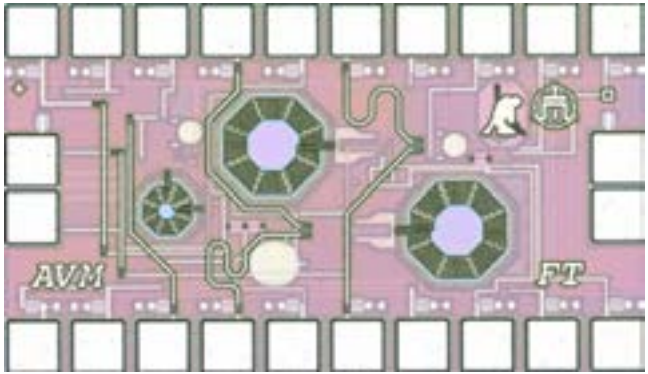
MICAS has investigated PMF for over ten years, increasing the data rate and distance with every new generation. Using a clever combination of PAM-4 signaling and two frequency bands, a data rate of 100 Gbps over 3 meters and 50 Gbps over 7 meters was achieved in 28 nm CMOS. This performance was obtained by finding the optimal trade-off between available bandwidth, channel dispersion, and linearity limitation of the circuits and the dielectric waveguide. The results of this research were presented at RFIC2023.





### Schottky photodiodes enabling unprecedented optical applications in silicon technologies

We proposed using Schottky photodiodes to detect light instead of typical pn-photodiodes. Such Schottky photodiodes are sensitive to light for which silicon is transparent, namely for wavelengts longer than ~1 µm. This allowed us to implement a single-chip 1340/1550 nm optical receiver in standard CMOS. Recently, we are using such Schottky photodiodes for clocking applications. The narrow-band nature of such applications allows us to suffer less from the low response from the integrated Schottky photodiodes. A test chip has been realized implementing an injection-locked oscillator controlled by the current from an integrated Schottky photodiode.




# Contact

## Wireline and Optical circuits

**Prof. P. Reynaert**
patrick.reynaert@kuleuven.be

**Prof. F. Tavernier**
filip.tavernier@kuleuven.be

"MICAS has a leading role in the field of Polymer Microwave Fibers, by pushing the boundaries of both data rate and distance."

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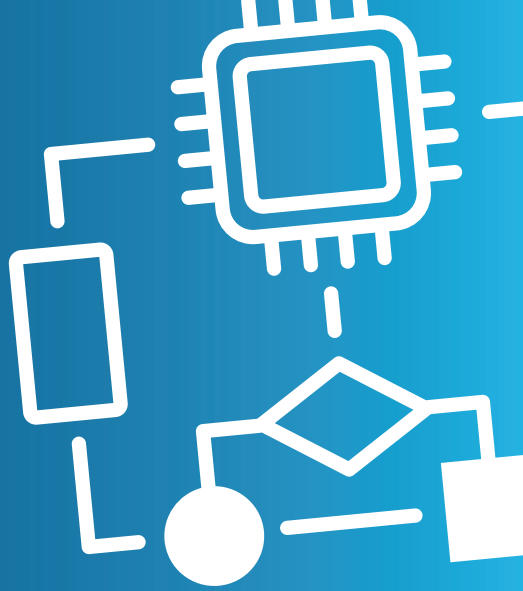
# Computer-aided hardware design and test



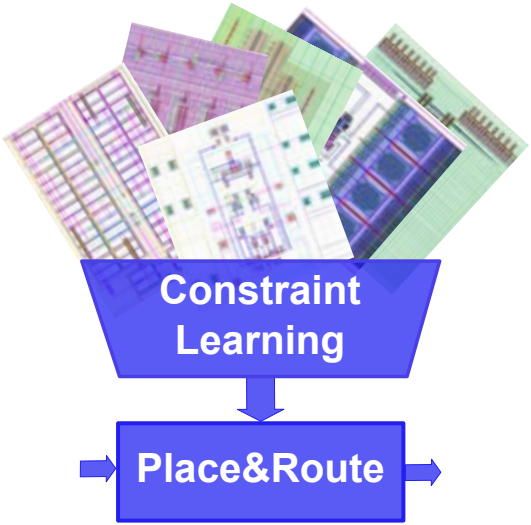
"MICAS performs research on innovative algorithms, modeling methods and design methodologies."

The design of electronic integrated circuits requires computer-aided design (CAD) tools for simulation, design and test. For many decades, MICAS is performing research on groundbreaking innovative algorithms, modeling methods and design methodologies to address emerging problems not (yet) covered by commercial CAD tools. These include the accurate modeling and efficient simulation of emerging phenomena in advanced as well as novel technologies, such as the stochastic modeling of time-dependent aging phenomena in deeply scaled CMOS, or the modeling and simulation of emerging quantum devices together with their drive control and readout circuitry. In addition, innovative methods for the design and layout optimization and automated synthesis of analog, mixed-signal and RF circuits have always been and remain a focus point of the MICAS research. In addition to powerful optimization methods, disruptive techniques from machine learning and artificial intelligence provide an avenue to increase the capabilities for the automated synthesis and verification of integrated circuits. Finally, MICAS explores pioneering algorithms and design-for-test techniques to boost the effectiveness of analog/mixed-signal test programs and to automatically generate test programs with a higher test coverage in a shorter time, both for hard as well as latent defects.

# 2023 highlights on computer-aided hardware design and test

### ERC project AnalogCreate: AI/machine learning methods for analog/ mixed-signal integrated circuit synthesis and test

Prof. Gielen's AnalogCreate ERC project is getting up to full speed. Despite the progress in CAD methods over the past decades, the design and test of analog/ mixed-signal ICs in industry still largely occurs manually by designers, resulting in long and error-prone design and test development times. Supported by the ERC Advanced Grant AnalogCreate, a large research effort is taking place at MICAS to develop sophisticated algorithms based on techniques from machine learning and artificial intelligence, in combination with advanced optimization and stochastic methods. The goals are the more efficient automated design and layout synthesis of analog/mixed-signal ICs, the structural synthesis of novel circuit topologies as well as the more effective automated verification of analog circuit designs. Key is the self-learning of constraints from example designs and layouts created by experts. Also, novel test methods are being explored using machine learning techniques to boost test coverage. First publications are on their way.

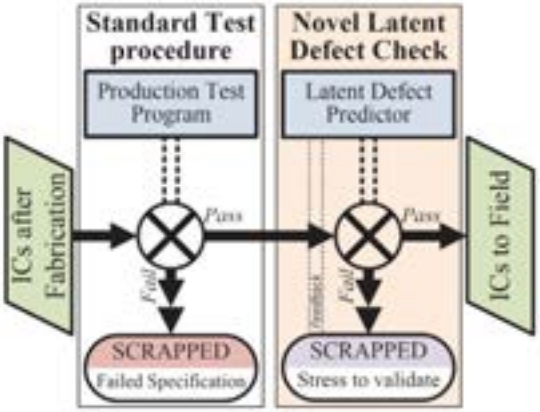



### Modeling of stochastic aging phenomena in advanced nanometer CMOS

Shrinking reliability margins have created an increasing demand for circuit aging simulations, which enable product reliability assessment before design tape-out. MICAS and imec are performing a detailed study to properly model the stochastic aging phenomena in advanced nanometer CMOS technologies and their impact on circuit performance. Models and simulations are validated experimentally by comparison with measurements of actual circuits such as amplifiers and ring oscillators. First results have been presented at IRPS 2023.

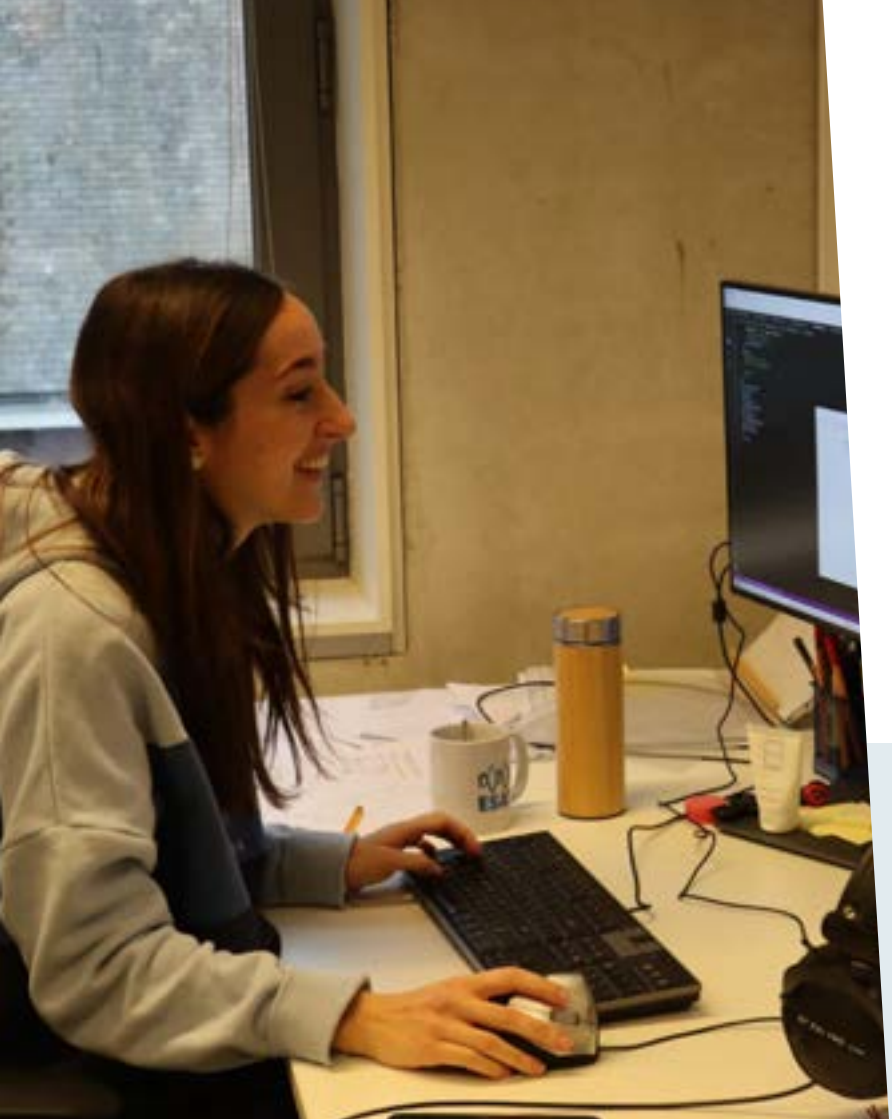
### Testing of quantum qubits: matching the behavior at room and cryogenic temperatures

Quantum computers aim at solving computationally hard tasks exponentially faster than classical computers. Today's qubits, however, operate at cryogenic temperatures. Testing the correct functioning of the qubits at such temperatures, however, is extremely expensive in time and cost, not only due to the required equipment and the long cool-down time, but also due to the limited number of packaged devices that can be tested in a single cool-down cycle. Therefore, MICAS and imec are carrying out research to find test routines for high-volume room-temperature screening of spin qubit arrays, by searching for device metrics that are measurable at room temperature (or just below) and that serve as good predictor for the qubit's performance at cryogenic temperatures. Initial experimental results for spin qubits and Single Electron Transistors (SETs) have been presented at the 2023 European Test Symposium and the 2023 International Test Conference.




### Methods and models for latent defect detection in analog/mixed-signal ICs

Safety-critical applications like automotive require test escape rates well below the 10-ppb level for their integrated circuits. For a decade now, MICAS has been working towards this goal, in collaboration with onsemi Belgium, exploring new test metrics, proper fault models, novel design-for-test methods and circuits, innovative test analysis methods and pioneering test generation algorithms, etc. With these improvements being transferred towards industrial practice, the biggest challenges currently being addressed are the increased coverage of latent defects as well as reducing the long lead time for analog test program development. By innovatively applying machine-learning-based classification to the outputs of industrial test programs, highly increased latent defect detection rates have been obtained. An approach using support vector machines (SVMs) has been demonstrated to increase latent defect detection from 58.4% up to 95.5%, at an additional yield loss of only 0.8%. These results have been published in IEEE Transactions on Computer-Aided Design (TCAD). The latest research in this area focuses on speeding up the analog test development using analog IP blocks and a defect-oriented BIST framework.



# Contact

Computer-aided hardware design and test

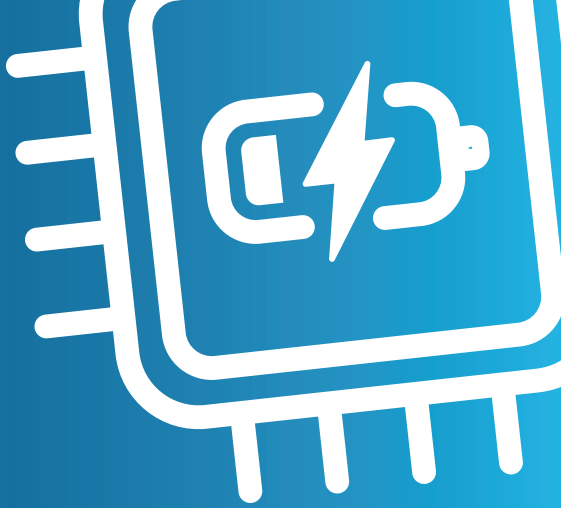
**Prof. G. Gielen**
georges.gielen@kuleuven.be

"We target the automated design and layout synthesis of analog/mixed-signal ICs, the creation of novel circuit structures, as well as a more effective automated verification and test generation for analog circuits."

## Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

# Ultra-low-power digital SoCs and memories

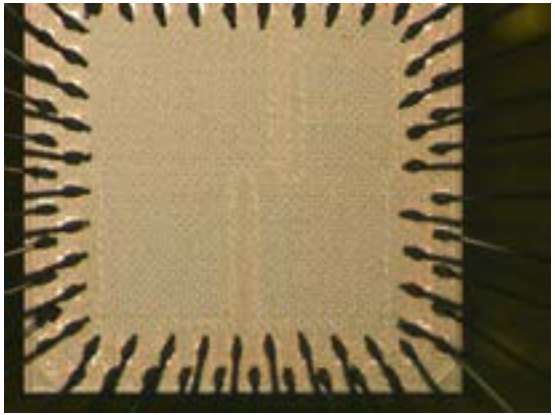


## “Exploring new digital design techniques and architectures to increase energy efficiency in digital processors”

Further evolution of applications in robotics, autonomous vehicles or biomedical wearables rely on ultra-high energy efficiency of the electronics circuits they encompass, while also requiring a large degree of flexibility and programmability. The deep-submicron evolution of silicon technology does not favor low-energy design, due to the ever increasing leakage and technological variability on the one hand, and the system complexity on the other hand.

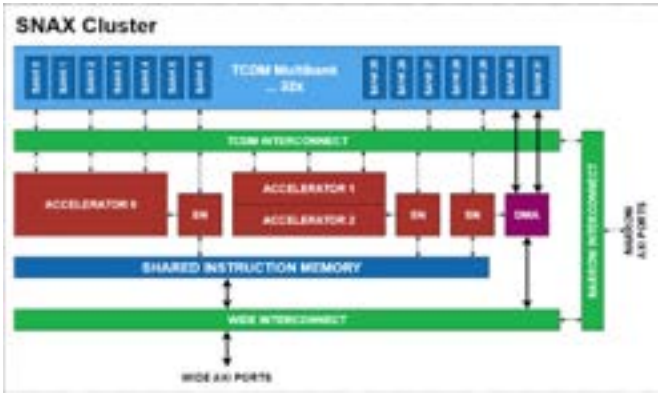
We reached the point where the classical remedies, e.g. multi-$V_T$ libraries or margined corner-based design, no longer suffice. Also in 2023, MICAS has been exploring new digital design techniques and architectures to increase the energy efficiency in digital circuits, ranging all the way from low-power memories to flexible customized compute fabrics.

# 2023 highlights on ultra-low-power digital SOCs and memories



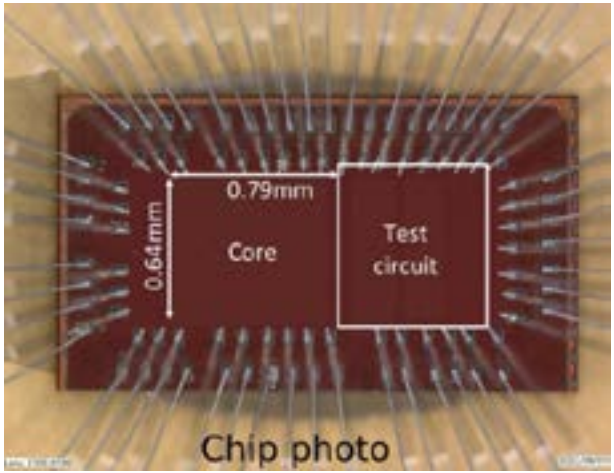
### Ultra-low-power memory design techniques

Designing ultra-low-power SRAM is a big challenge. Getting the leakage down is the message. When accessing the memory, we use high-VT cells and a relatively high supply. However, in retention mode the power supply should be reduced as much as possible. In our recent SRAM design, we showed that by including some redundancy and a relatively simple error correction code we can reduce the power supply beyond the point of first failure or the point of first forget for a memory. In this way we significantly reduce the leakage while keeping the area overhead to a minimum. All this was implemented in a prototype ultra-low-power 1 MHz, 256 Kb, SRAM memory that we call BRUTUS, pictured above, and published in Transactions on Circuits and Systems.




### Flexible RISC-V based multiaccelerator fabrics with SNAX

We are advancing energy-efficient hardware processing with the development of a RISC-V-based multi-accelerator platform. Recognizing the limitations of a single, overly flexible accelerator for complex compute kernels, SNAX offers a template for seamlessly composing multiple hardware accelerators from both the hardware and software perspective. The hardware design template includes a Snitch core for control, a tightly coupled multi-banked memory interface, and a configurable interface definition between the controller core and accelerator(s), as well as between accelerators and the memory system. Software integration is backed by a close coupling to the MLIR open-source multi-level compilation framework. SNAX is undergoing testing and integration with a first set of Gemm accelerators, showcasing its adaptability to different accelerators and compiler optimization passes.




**Digital in-memory computing at 0.36 TOPs/mm² and 256 kB/mm²**

Digital in-memory compute (DIMC) comes with large efficiency benefits compared to traditional digital architectures, while it brings robustness against variability and ease of integration into the digital design flow compared to analog in-memory compute. We realized a chip that overcomes the traditional DIMC bottlenecks, such as a low area efficiency, and the need to modify the bit-cell. This enables us to upscale the DIMC accelerator to large macros for practical tasks. The chip, implemented in TSMC 16 nm technology, achieves 23.8 TOPs/W for 8b MAC operation, a storage density up to 256 kB/mm² and 0.36 TOPs/mm² compute density. The results were presented at ESSCIRC 2023.

# Contact

## Ultra-low power digital SoCs and memories

**Prof. W. Dehaene**
wim.dehaene@kuleuven.be

**Prof. M. Verhelst**
marian.verhelst@kuleuven.be

"The introduction of AI techniques makes the power consumption challenge in IoT applications even bigger. The advanced logic and memory designs of MICAS will help to solve this challenge and unblock the road to a smarter, safer and more sustainable society."

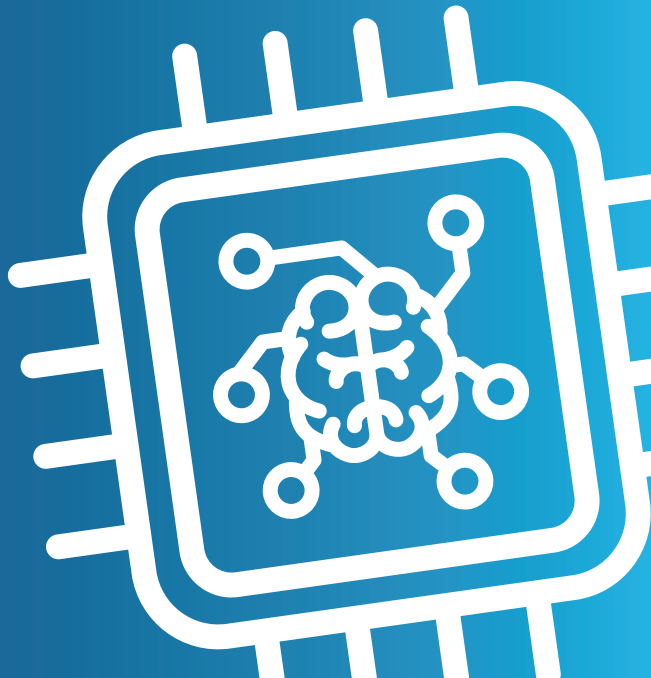
### Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

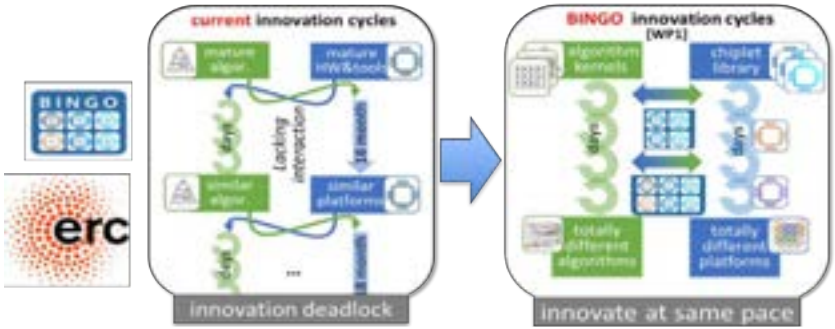
# Hardware-efficient AI and ML

"The scientific challenge in enabling artificial intelligence in the edge and the cloud, is to strike the right balance between hardware customization and model flexibility."

Artificial Intelligence (AI) and Machine Learning (ML) are becoming indispensable in our everyday life: from clever chatbots like chatGPT, over autonomous vehicles, to wearable health and activity monitoring systems. The impressive progress in this field, however, comes with drastic increases in model sizes and complexities. Execution efficiency can be obtained by customizing processor architectures to the models of interest. Yet, the speed at which new models emerge, impede such tight co-optimization, and require the hardware platforms to be flexible towards future developments. The challenge is hence to strike the right balance between customization and flexibility. In 2023, our MICAS team has continued to work on several innovations towards this goal.



# 2023 highlights on hardware-efficient AI and ML



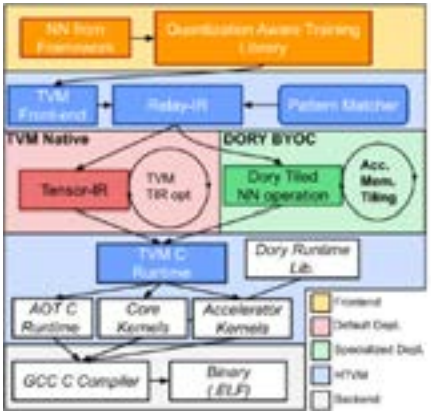

*The vision of the BINGO project*

### Kick-starting the Bingo ERC project!

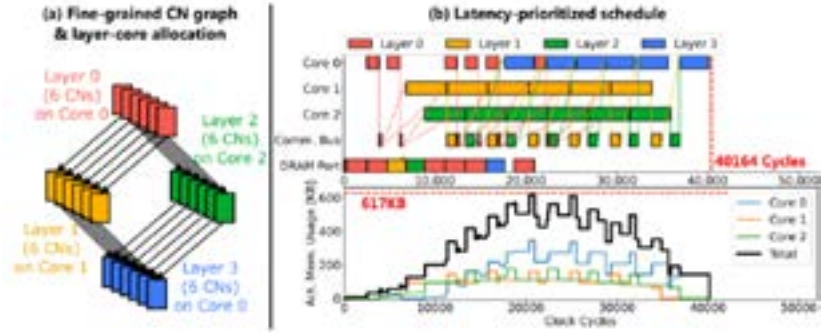
In 2023, Prof. Verhelst's BINGO ERC project launched. BINGO tackles the problem of the discrepancy between the slow development cycle of processor chips (many months to years) and the high-pace evolutions of machine learning algorithms (hours to weeks). This bottleneck is also known as the "hardware lottery", and holds back innovation, severely impacts embedded AI execution efficiency, and narrows the market to a few large companies. The BINGO vision to break this innovation deadlock is to enable heterogeneous compute platform customization for a given AI workload in a matter of days (100x faster), through rapid selection and assembly of prefabricated co-processor chiplets. A new team at MICAS will enable that vision in the coming five years of the BINGO project.

### Sensor processing with spiking neural networks and continual learning

Traditional approaches for processing sensor data through deep neural networks are energy- and area-hungry. Exploiting the spiking and event-based nature of the signals, spiking neural networks (SNNs) in combination with proper signal preprocessing are significantly more energy-efficient in their implementation, making them affordable for local in-sensor processing and a better solution for many IoT applications and edge devices. The feasibility and benefits have been demonstrated for the real-world applications of SNN-based processing of radar signals for gesture recognition and object avoidance during autonomous drone navigation. Recent work has added bio-inspired continual learning to the SNN using Spike-Timing-Dependent Plasticity (STDP). The approach does not require any offline training, but continuously learns from the input data via STDP. This has been demonstrated for detecting people on the fly in event-based camera video data mounted on the drone. The work has been published in the ICRA 2023 conference.




*The HTVM compilation flow*




*Efficiently mapping AI workloads on heterogeneous architectures with Stream*

### Heterogeneous hardware accelerators and compilers

The domain of machine learning is recently seeing a strong diversification in terms of algorithms. Neural networks are increasingly combined with other techniques, such as probabilistic graphical models. In MICAS, we are also developing accelerators for these workloads, as well as ways to efficiently integrate them into heterogeneous multi-core platforms, supported by custom compilers. In 2023, we taped out a 16 nm accelerator supporting graphical models, and a digital in-memory compute accelerator. We moreover presented a customizable compiler framework in TVM (HTVM, DAC2023), and are currently migrating our compilation flow to MLIR.

### Improved Stream and ZigZag-IMC for exploring multi-accelerator platforms.

When running machine learning workloads on heterogeneous multi-accelerator systems, the design space as well as the scheduling or mapping space is enormous. However, it is important to explore this complete space, as savings of more than one order of magnitude of energy efficiency and latency can be obtained by optimizing across the stack. MICAS previously developed the ZigZag and Stream tools to enable this. In 2023, Stream was further enhanced to efficiently explore larger models, while ZigZag was extended with support for in-memory compute accelerators. Together, they allow to explore fine-grained, layer-fused scheduling of very heterogeneous AI accelerator platforms. All tools are available in open-source at https://github.com/KULeuven-MICAS.


# Contact

## Hardware-efficient AI and ML

**Prof. M. Verhelst**
marian.verhelst@kuleuven.be

**Prof. W. Dehaene**
wim.dehaene@kuleuven.be

**Prof. G. Gielen**
georges.gielen@kuleuven.be

"Customized multi-accelerator architectures are driving the rapid evolutions in artificial intelligence. MICAS is proud to perform at the forefront of this trend and keeps pushing the boundaries of the SotA."

### Interested to read more?

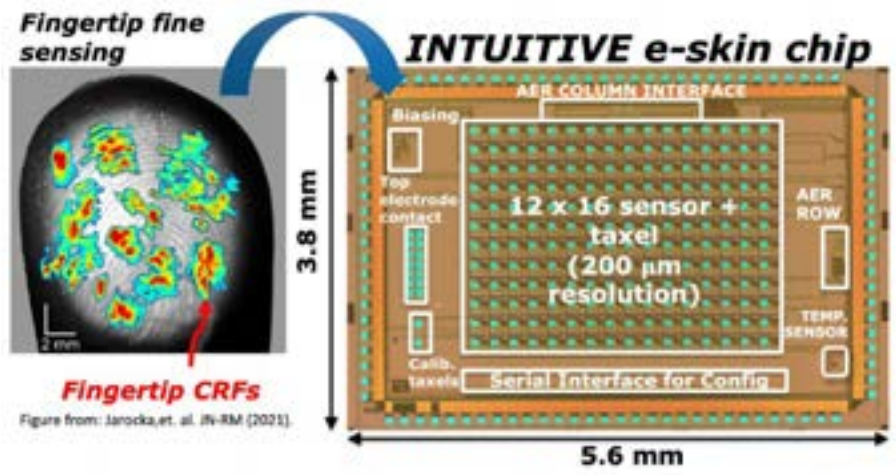
Check out our website for a detailed overview of all research topics in this domain.

# Biomedical circuits and sensing interfaces

"The research at MICAS explores innovative chip implementations and hardware solutions for biomedical applications and sensing readout."

Sensors connect the physical world with the electronics world, and are therefore crucial building blocks for many applications, like multimedia, augmented/virtual reality, modern cars, entrance control, robotics, etc. Enabled by the increasing capabilities of (wireless) communications, like the Internet of Things, distributed sensing devices have recently become key to constructing smart system applications, like smart mobility, smart cities, smart manufacturing, smart farming, etc. Challenges in the design of the sensing readout involve the relentless reduction of the power and silicon area, while achieving increased performances in terms of sensitivity or dynamic range. The large amount of data generated in the sensing also calls for increased local data processing or computation "in the edge" to limit the communication cost. An application field that has always been of special interest in MICAS is biomedical. Electronics can enable better diagnosis, monitoring, therapeutics, and more personalized medicine in general, saving and/or improving lives. Biomedical devices today range from large to handheld equipment and from wearables to implantables and ingestibles. Electronics not only allow for miniaturization but also add intelligence and customization capabilities. For several decades and years to come, the research at MICAS has been exploring improved chip implementations and innovative hardware solutions for biomedical applications, often in collaboration with medical doctors from the university hospital.

# 2023 highlights on biomedical circuits and sewnsing interfaces



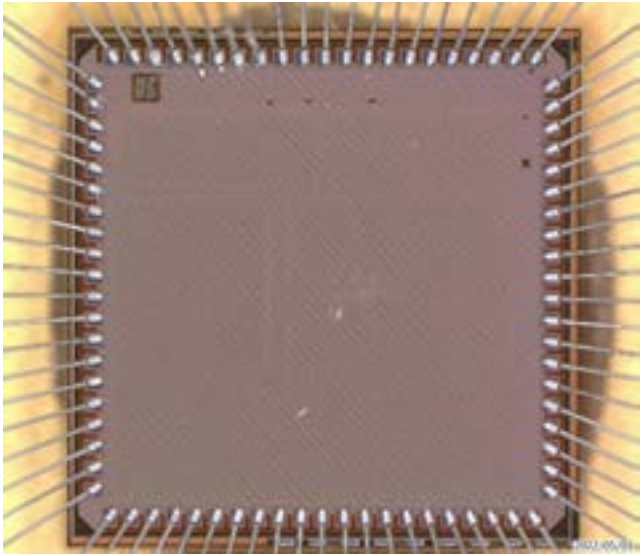

**A fingertip-mimicking high-resolution e-skin readout chip**

Electronic skin (e-skin) solutions are important for the design of prosthetic or robotic hands with human-like tactile capabilities. MICAS has designed the INTUITIVE taxel readout chip in 0.18 µm CMOS technology that achieves a record-high spatial resolution of 200 µm, comparable to human fingertips. A key innovation is the integration on chip of a 12x16 taxel array with a per-taxel signal conditioning frontend and spiking readout combined with embedded neuromorphic first-order processing through Complex Receptive Fields. The chip incorporates a polyvinylidene fluoride (PVDF)-based piezoelectric sensor layer.

Experimental results show that Spiking-Neural-Network-based classification of the chip's spatiotemporal spiking output for input tactile stimuli such as texture and flutter frequency achieves excellent classification accuracies up to 99%, even when using a small low-bit SNN. The chip consumes a state-of-the-art per-taxel power of 12.33 nW. It has been presented at the 2023 VLSI circuits conference. An end-to-end architectural exploration and optimization environment for such sensing applications has been presented at the DATE 2023 conference.

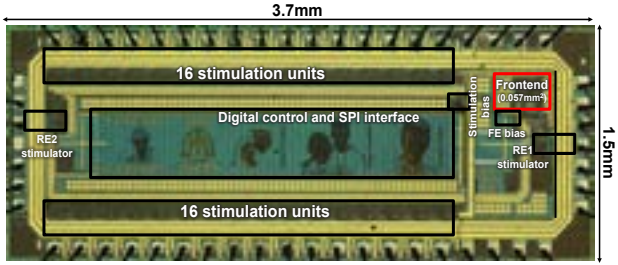
### Circuit innovations for biomedical sensing readout

MICAS continuously explores and proves the feasibility of novel circuit innovations for biomedical sensing readout applications. In 2023, a high-speed readout for nanopore-FET (NPFET) sensor arrays has been developed, intended for high-throughput DNA or protein sequencing. The readout interface utilizes a novel architecture that can simultaneously perform recording and automatic background calibration to compensate for offset and drift of the individual NPFET threshold voltages. An 8-channel chip has been prototyped in 0.18 µm CMOS and published in the IEEE Transactions on Circuits and Systems I. A second design is an online spike-sorting chip in 22 nm FDSOI CMOS, able to process neural signals from 384 channels with software-comparable accuracy. To handle the trade-off between hardware resources and real-time performance, optimized spike detection, feature extraction and on-chip sorting are implemented, requiring an area of 0.0013 $mm^2$ per channel, a power consumption of 1.78 µW per channel, a latency of 33.9 µs, and a spike sorting accuracy of 97.7% without clustering pretraining. The work has been published in the ISSCC 2023 conference and subsequently in the IEEE Journal of Solid-State Circuits.



### Proof of concept design for a visual prosthesis chip

How fantastic would it be if we could at least partially restore the vision of blind people. Together with our partner ReVision Implant, MICAS is working towards this goal. We developed a 16-channel proof-of-concept chip for a visual prosthesis. The challenge in such a stimulator is to guarantee charge balance over a current range up to 100 µA and a voltage range up to 10 V. The chip we presented at BioCAS and later published in Transactions on Biomedical Circuits and Systems shows that this is possible in 65nm CMOS with 16 channels as proof of concept. We are now working on a full-blown stimulator chip with 256 channels, wireless downlink and full digital programmability.




### SCATMAN: a fully integrated chip solution for neural monitoring and stimulation in stroke-induced cavities

Closed-loop neuromodulation (with both monitoring and stimulation) is emerging as a more effective solution for the treatment of neurological symptoms, such as the treatment of abnormal neural behavior near stroke-induced brain cavities. A challenge is the ability to continuously record brain activity during electrical stimulation, due to the large artifacts that can saturate the sensitive readout circuits. A proof-of-concept chip in 180 nm CMOS has been developed containing multi-channel stimulation and a multi-channel multiplexed readout frontend with rapid artifact recovery that needs to be combined with backend linear interpolation to reconstruct the artifact-corrupted signal features. The chip contains time-domain conversion using a novel 13-bit incremental ADC and requires a record minimum area of only 0.0018 $mm^2$ per channel, while consuming only 4.51 µW per channel. The work is an ideal candidate for integration in high-channel-count true closed-loop neuromodulation systems and has been presented at the BioCAS 2023 conference.

# Contact

## Biomedical circuits and sensing interfaces

**Prof. W. Dehaene**
wim.dehaene@kuleuven.be

**Prof. G. Gielen**
georges.gielen@kuleuven.be

"Challenges in the design of the sensing readout involve the relentless reduction of the power and silicon area, while achieving increased performances in terms of the sensitivity or dynamic range."

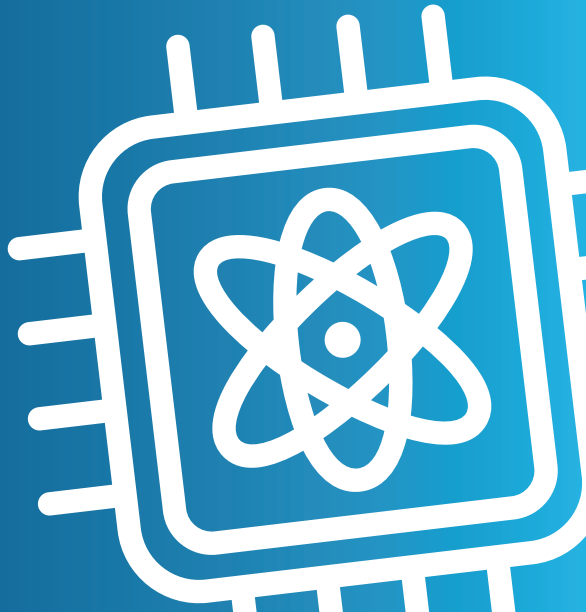
### Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

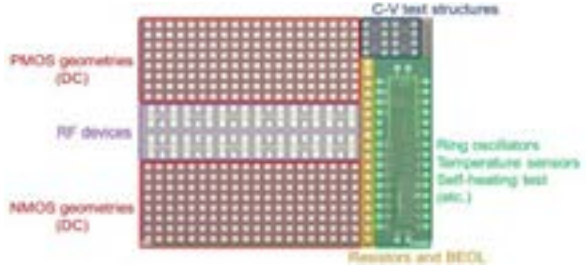
# Quantum and cryogenic circuits

"Solid-state circuits to control and observe a growing number of quantum devices will be essential."

Quantum technologies, including computing, sensing, communications, information technology, and security, are rapidly emerging thanks to the combination of future challenges in these domains and recent advancements that enable quantum technologies to provide an answer. Solid-state circuits to control and observe the growing number of qubits will be essential in successfully realizing such technologies. Since most quantum technologies rely on deep cryogenic temperatures, circuits must also work at those temperatures to ensure compact, reliable, and, especially, scalable systems. The Einstein Telescope, the next-generation gravitational wave detector currently under development, also requires cryogenic operation and, thus, cryogenic circuits. MICAS is involved in all these initiatives, and it also has invested in the necessary cryogenic measurement infrastructure.



# 2023 highlights on quantum and cryogenic circuits




### Our custom cryogenic transistor model

The design of optimized low-power cryogenic chips depends heavily on an accurate transistor model. Unfortunately, the foundry models are not valid at cryogenic temperatures, resulting in the need for over design, or, even worse, failed chips. Therefore, we have developed our own custom cryogenic transistor model, based on accurate transistor measurements and modifying the model parameters in the PDK. This model allows us to develop cryogenic chips with a better accuracy. The photo above shows one of our test chips containing numerous transistors for cryogenic characterization.

### Cryogenic mixed-signal circuits for high-speed digitization

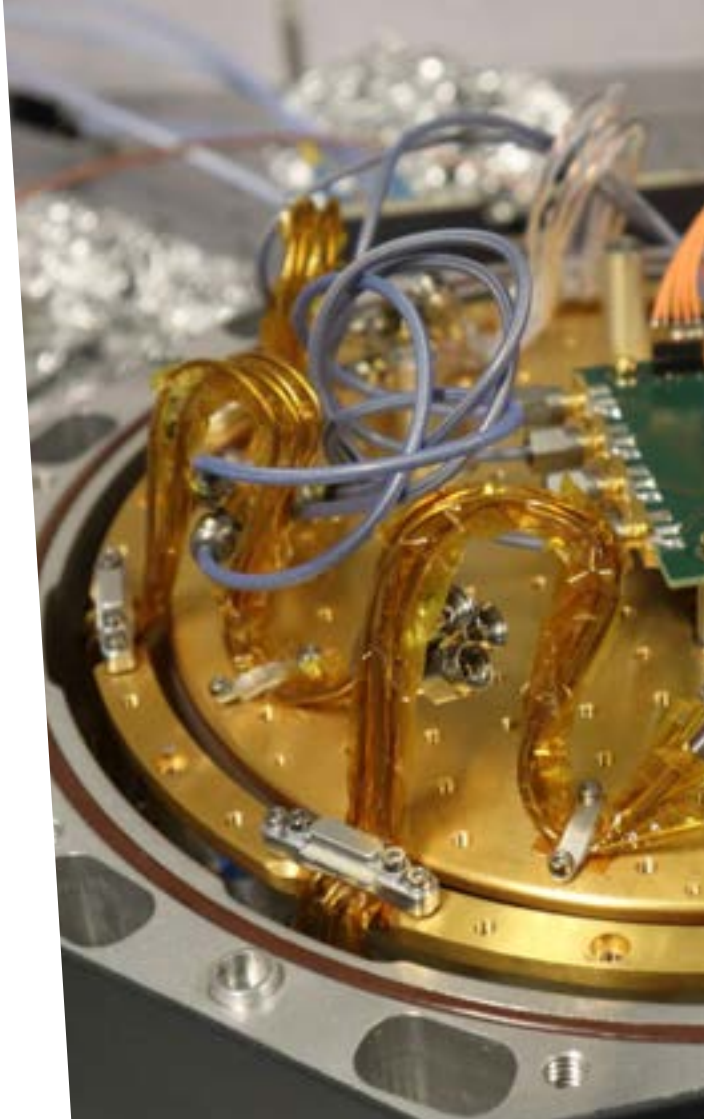
Based on our cryogenic transistor models, we have started developing cryogenic comparators, essential building blocks in an ADC, which is a critical component in the readout of qubits in a quantum computer. Additionally, we have taped-out our first cryogenic ADC. This ADC has been conceived from the ground up to tackle the specific benefits of the cryogenic environment, for example the low thermal noise, while avoiding the traditional pitfalls, for example the increased threshold voltage.

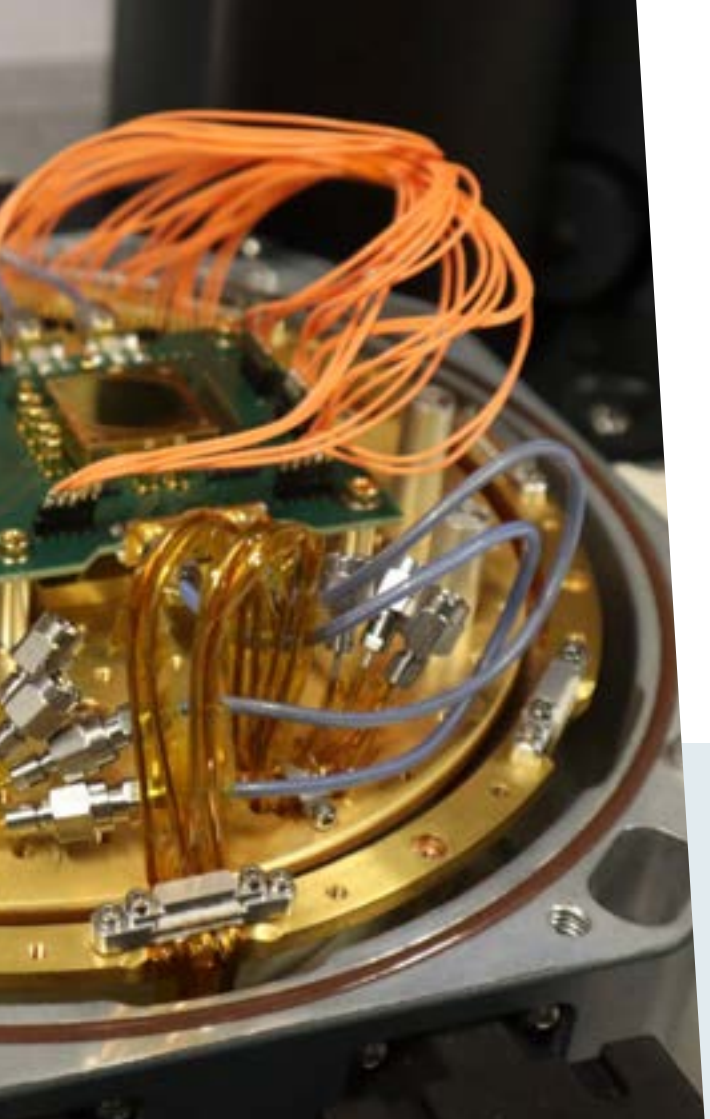
### Cry-CMOS multiplexer for qubit control at millikelvin temperatures

Large-scale superconducting quantum computers require the high-fidelity control and readout of large numbers of qubits at millikelvin temperatures, resulting in a massive input–output bottleneck. To address this, a cryo-CMOS multiplexer, allowing to drive and read out multiple qubits, has been designed and measured to operate below 15 mK with minimal channel cross-coupling. Using the multiplexer, single-qubit gate fidelities above 99.9% — that is, above the threshold for surface-code-based quantum error correction — can be achieved with appropriate thermal filtering. The joint MICAS-imec work has been published in Nature Electronics.

### Commissioning of our cryogenic lab equipment

Characterization of chips at cryogenic temperatures, requires dedicated cryogenic fridges. Since 2022, we have a Montana Instruments S200 general purpose cryostation. It has a sizeable sample space with a diameter of 20 cm and a height of 7.5 cm. It has been custom retrofitted to perform fA current measurements. In 2023, we acquired a Lakeshore CRX-4K cryogenic probe station. Both systems are closed-cycle systems and can cool down to approximately 4 K. They serve complementary measurement needs.





# Contact

## Quantum and cryogenic circuits

**Prof. F. Tavernier**
filip.tavernier@kuleuven.be

"Quantum and cryogenic circuit design provides exciting new challenges for proven and scalable CMOS technologies."

### Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

# Educating for excellence

We train and guide talented **PhD** and **postdoctoral students**, to become trendsetters in micro- and nanoelectronics.

We involve **bachelor** and **master students** who are passionate about the world of chip design in our projects.

# Training experts at the bachelor, master, PhD and continued-learning levels

## Bachelor

MICAS supports bachelor education in Electrical Engineering at KU Leuven. In this curriculum, students are trained in the broad range of electrical engineering subjects, and are learning the fundamentals in the field, with a strong mathematical foundation. The MICAS professors offer education in electronic circuit design and digital implementation. Every year, about 400 new bachelor students join this program.

## Master

Within the master in Electrical Engineering at KU Leuven, one of the tracks specializes on chip design, training tomorrow's IC designers. Master students enrolled in the program are trained by the various MICAS professors on all different aspects of chip design, ranging from analog and mixed-signal design, over RF and mm-wave circuits, to digital implementations and processor architectures as well as CAD. Every master student also performs a deeper study on one subject in her/his master thesis, and as such already gets a taste of the MICAS research culture.

## PhD

MICAS houses more than 70 PhD students, maturing to become true experts in their fields. An important aspect of their work is to explore innovatively new circuit solutions, but also to validate these concepts experimentally through actual chip implementations. In addition, the PhD students are not only trained to excel technically, but they also get educated in effective communication, creativity, teamwork, paper writing, and student supervision. As such, we are proud to train the change makers of the future in the world of chips.

## Continued-learning micro-credentials

In 2023, and within the frame of the EU Chips Act and the upcoming national Competence Centers, MICAS has launched a series of micro-credential courses together with several leading companies in the field. These micro-credentials enable both students and professionals to up-skill and re-skill themselves in the field of analog and digital chip development. The courses cover a range of industry-relevant competences that allow both experts and novices to start or continue a career in chip design and development.

## NEW MICRO-CREDENTIAL COURSES ON CHIP DEVELOPMENT

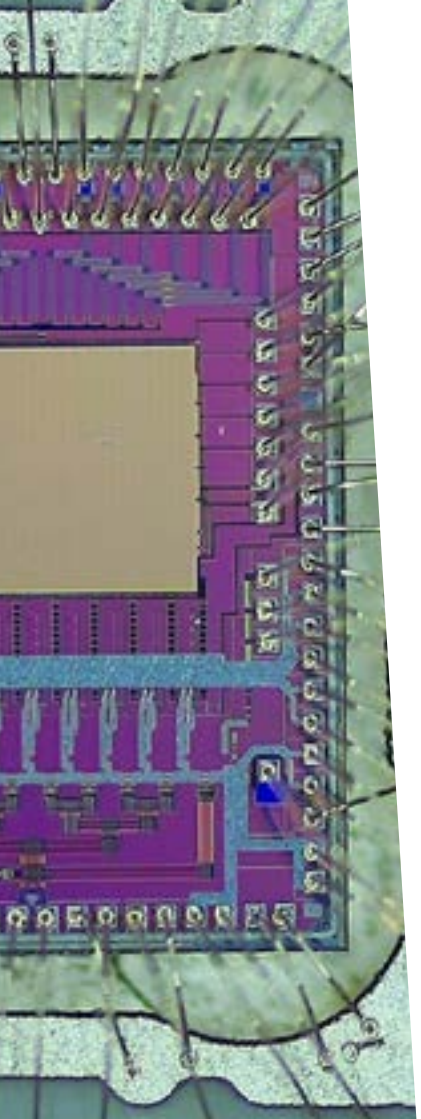
In response to the critical shortage of skilled engineers in semiconductor Integrated Circuit (IC) design and layout, a new initiative has been launched by professor Patrick Reynaert of KU Leuven in collaboration with several leading semiconductor companies in Flanders, Belgium. Flanders boasts a myriad of commercial enterprises at the forefront of cutting-edge chip design technology. These companies play pivotal roles in various electronic applications, spanning automotive, medical, industrial, consumer, data center, optical, and space industries. Despite their ambitious growth plans, the semiconductor industry worldwide – and also in Flanders – faces a significant hurdle: a shortage of qualified engineers in IC design and layout.

To address this challenge head-on, professor Reynaert's recent initiative introduces comprehensive courses, called micro-credentials, designed to coach individuals into proficient 'chip developers'. This program provides students and professionals with specialized skills essential for different semiconductor industry roles. Crucially, the courses are not just theoretically driven; they are developed and taught by seasoned experts from Flanders' leading semiconductor companies. Participating firms include BelGan, Caeleste, Cyient, easics, iCana, ICsense, imec, Melexis, Omnivision, and Sofics. This collaboration ensures that students gain practical insights, real-world perspectives, and industry-specific knowledge directly from those shaping the landscape.

A first course in early 2024 covers the skills required to draw the layout of analog chips, including imagers, ESD protection and high-speed aspects. This course targets a wide range of profiles interested to learn and understand the art of analog layout, either to become a layout engineer or just to learn the challenges and good practices of analog layout. A second course will go in-depth in the topic of digital verification. A third course will cover GaN, a promising technology for power management and RF circuits. It will be a full-week course and covers both the technology aspects as well as some of the design aspects. We plan to offer more courses later on together with both our local and international partners.

The course is supported by Continue, the online platform for lifelong learning from the KU Leuven Association.

More info:



## What appeals students at MICAS?

Why do PhD and master students like studying and working at MICAS? What makes MICAS/ KU Leuven a good place for them? What opportunities does it bring?

We asked them these questions, which resulted in a variety of answers ...

"MICAS gives you the opportunity to go through the entire chip design cycle from idea, design, manufacture to actually measure your own integrated circuit(s)."

**Thomas**

"A unique mixture of creativity, freedom, and knowledge topped with some funny craziness."

**Tim**

"You can work with many international researchers having various backgrounds in the field of electronics. A lot of opportunities to design a chip in advanced technologies, to collaborate with world-wide companies and with imec."

**Kodai**

"At MICAS, I experienced unprecedented creative freedom, allowing me to substantially broaden my knowledge, enhance my skillset, and engage in the most advanced research within my capabilities, all within a supportive and enjoyable community of like-minded individuals."

**Carl**

# Inspiring society

Besides education and research, MICAS also sees it as its core task to inspire others.

This includes inspiring youngsters towards a career in STEM or micro-electronics; inspiring society towards the opportunities that come from ubiquitous electronics; and being a continued source of inspiration for our alumni to keep developing electronics in applications that matter. We are proud to discuss some recent initiatives in these areas.

> "Making society aware of the importance of microelectronics and resulting opportunities."

> "Enthusing others to actively participate in the shared mission of using STEM and micro-electronics towards a better society."

## OUTREACH

We not only publish our research output in peer reviewed scientific journals, but we also write articles for magazines with a broader audience. In this way, we inform the more general public about our realizations and about the opportunities of our research.

We also use other channels to reach out to a broad audience, from television to social media, live science debates and podcasts. Prof. Marian Verhelst is a regular guest in the monthly science podcast "Nerdland", which discusses (in Dutch) the scientific breakthroughs of the month to non-experts. From 2020 to 2023, this podcast consistently ranked within Spotify's top 3 of Flanders most popular podcast.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## STEM

STEM disciplines (**S**cience, **T**echnology, **E**ngineering and **M**athematics) struggle to attract sufficient students to cover the need of the job market. One of the root causes of this problem seems to be the difficulty to link the abstract study fields of science and mathematics with the practical application and relevance of these disciplines in our day-to-day lives.

To overcome this, MICAS leads multi-partner projects like the educational network 'iSTEM' and InnovationLab. With these projects, we aim to not only enhance the STEM literacy of youngsters, but also to improve their attitude towards STEM and its role in society.

**InnovationLab:** The link between technology and the impact on people's daily life takes a central role in the vision of InnovationLab, which offers fully developed STEM projects in which students tackle a societal challenge (https://eng.kuleuven.be/innovationlab/). Each InnovationLab project can be carried out at the secondary school itself, by the school's own teachers, using the material provided by InnovationLab. On these project days, students can experiment, investigate, and practically engage themselves in real engineering tasks.

**iSTEM:** The activities of iSTEM range from secondary-school teacher professionalization and inspiration to coaching. On the website (www.istem.be) teachers find, among other tools and inspiration, more than 50 projects which they can adapt to their everyday class practice (creative commons license). On top of the intensive courses and workshop teachers can attend weekly iSTEM nocturnes, where each time one of the projects is highlighted. On top of the tailor-made coaching activities of teacher design teams, schools can now enroll in a comprehensive trajectory to strengthen their STEM education.

# Spin-offs

Disruptive research opens up new markets, not yet covered or under development in existing companies. This is where entrepreneurship within MICAS meets research. MICAS is very successful in this model, leading to the creation of on average one spin-off company every four years. The total amount of employment to date due to these spin-offs is over 300 full-time employees, mostly highly skilled IC designers and electronic-system engineers. Since most of these companies are located near KU Leuven, this creates a local Silicon Valley ecosystem in the Leuven area. These spin-offs regularly operate in close collaboration with KU Leuven and the MICAS researchers. Learn here about the most important news of 2023 from our spin-offs.


AnSem, a Cyient company, has established secure rooms and secure vaults to perform advanced technology node design (down to 3nm) in the following locations – Leuven (Belgium), Duisburg (Germany) and Hyderabad/Bangalore (India). This advanced setup will help the company to support state-of-the-art ASICs of tomorrow in the areas of 5G, IoT, Data Centers, etc. AnSem is one of the very few global technology companies that provide both Semiconductor Services and Solutions including Supply Chain Management.


In 2023, Hammer-IMS succeeded in opening a branch office in the United States to reach more customers in the American continent. Several new commercial projects have been set-up with industrial production facilities abroad, reaching far places like South-Korea and Australia. Hammer-IMS was involved in several commercial projects in the area of its new Edge-Vision-4.0-CURTAIN machine-vision technology.


MAGICS Instruments is a spin-off company of MICAS since 2015, specializing in the design of radiation-hardened, integrated circuits. They deliver customized state-of-the-art, radiation-tolerant electronics to their customers and they provide radiation qualification services on ASICs or commercial-off-the-shelf components. As such, they identify potential risks and improve reliability. The MAGICS Instruments technology is qualified under extreme radiation conditions. MAGICS Instruments is currently active in the following markets: space industry and high-energy particle physics.

ICsense celebrates 20 years of IC design. The company grew to 100 employees and expanded its design centre in Ghent. It has the largest fab-independent European IC design team with world-class expertise in analog, digital, mixed-signal and high-voltage design. ICsense invested in additional ATE capacity (mass production test equipment) and offers in-house wafer-probing. The company develops and supplies customer exclusive ASIC solutions for the automotive, medical, industrial and consumer market compliant with ISO9001, ISO13485, IEC61508-ISO26262.

Being part of the TDK group since 2017, ICsense develops custom chips for most major smartphone makers and works for the top-players in automotive. The majority of ICsense's business remains however outside of TDK. As a result of its strong company culture and reputation, ICsense is proud to have a +90% employee retention rate, which is among the highest in the IC design community worldwide.

MinDCet was founded in 2011, as a spin-off from the MICAS research group. MinDCet is an ISO9001 certified, fabless, mixed-signal IC design company, developing Power Management ICs. MinDCet develops highly/fully integrated and discrete DC-DC converters, motor drivers, high-speed GaN and laser drivers, control systems, class-D amplifiers, power and battery management. Currently, MinDCet is active in the following markets: automotive, industrial, aerospace & space, biomedical, high-reliability & harsh environments.

During 2023, Tusk IC prototyped their first internally developed beamformer chip for Satcom and 5G infrastructure applications. The chip measurements show excellent matching between simulation and measured results. In parallel, Tusk continued to deliver cutting-edge mmWave designs for their medical, communication and automotive clients. In November, Tusk IC joined Flanders Space, a cluster shaping the space economy in Flanders.

# MICAS team

MICAS is a close-knit, collaborative team of professors, researchers, and support staff, striving for excellence, “pushing ourselves to deliver the highest-quality performance in everything we do”

- **6 professors**, each excelling in his or her discipline, skills and expertise acquired at academic institutions, industrial multinationals, or a combination of both, domestically and abroad;
- **70 PhD** students and **postdocs**;
- **12 technical and support employees** to coach and help researchers on the use of design and measurement infrastructure, and to assist the whole team in matters related to HR, finance, IT, and tech transfer.

# Academic staff

## Wim Dehaene

**Main research topics:**

- Circuit-level digital design
- Low-power digital circuits
- Biomedical circuits
- Design in TFT technology

## Georges Gielen

**Main research topics:**

- (Beyond) CMOS analog and mixed-signal IC's
- Data converters and sensing interface circuits
- Analog/mixed-signal CAD tools and design automation
- Testing of analog/mixed-signal ICs

## Patrick Reynaert

**Main research topics:**

- Power amplifiers
- Mm-wave and THz CMOS circuit design
- High-speed and broadband circuits

## Michiel Steyaert

**Main research topics:**

- Power management and DCDC circuits
- RF CMOS and telecommunication circuits
- Wireline and optical communication circuits
- Analog signal processing and A/D and D/A converters

## Filip Tavernier

**Main research topics:**

- Circuits for optical communication
- High-speed wireline communication
- High-speed A/D and D/A converters
- Fully integrated power management
- Radiation-hard IC design

## Marian Verhelst

**Main research topics:**

- Chips for machine learning and AI
- Computer architectures
- Low-power, embedded processing
- Context-aware, ubiquitous electronics

# MICAS Emeriti

## Bob Puers

**Achievements:**

- Medical implants for monitoring and stimulation
- Sensors and actuators
- Silicon and polymer MEMS
- Biocompatible packaging and interconnection
- Biotelemetry and inductive powering

## Willy Sansen

**Achievements:**

- Analog circuit design expert
- Headed the MICAS group 20+ years
- Supervised 60+ PhD theses
- Received numerous awards and prizes
- Past-President of IEEE Solid-State Circuits Society

# PhD Graduates 2023

## Nimish Shah

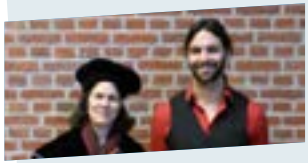
**Embedded Execution of Irregular Dataflow Graphs: Hardware/Software Co-optimization for Probabilistic AI and Sparse Triangular Systems**

Promotor: Prof. Marian Verhelst (promotor), Wannes Meert (co-promotor)

## Vikram Jain

**Towards Heterogeneous Multi-core Systems-on-Chip for Edge Machine Learning**

Promotor: Prof. Marian Verhelst (promotor), Prof. Peter Karsmakers (co-promotor)



## Jaro De Roose

**Ultra Low Power Adaptive Sensor Nodes**

Promotor: Prof. Marian Verhelst

## Koen Goetschalckx

**Optimizing Embedded Vision Efficiency across the Hardware-Dataflow-Algorithm Stack**

Promotor: Prof. Marian Verhelst

## Maarten Herbosch

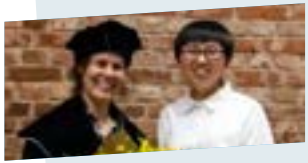
**Intelligent Contracting: Legal Aspects of the Precontractual Use of Artificial Intelligence**

Promotor: Prof. Bernard Tilleman (promotor), Prof. Georges Gielen (co-promotor)

## Thomas Bos

**Ultrasonic Communication Through the Human Body: Channels, Modems and Hardware for Ultrasonic Communication Connections**

Promotor: Prof. Wim Dehaene (promotor), Prof. Marian Verhelst (co-promotor)



## Linyan Mei

**Design Space Exploration of Deep Learning Accelerators**

Promotor: Prof. Marian Verhelst

## Valdrin Qunaj

**mm-Wave Power Amplifiers for Wireless Communication in Advanced Semiconductor Technologies**

Promotor: Prof. Patrick Reynaert

## Lynn Verschueren

**Design, Driving, and Compensation for High-Resolution Active Matrix Displays**

Promotor: Prof. Wim Dehaene (promotor), Prof. Jan Genoe (co-promotor)

## Xiaohua Huang

**Multiplexed Acquisition Systems for High-Resolution Brain Mapping and Emerging Brain-Machine Interfaces: Where CMOS Meets TFT**

Promotor: Prof. Chris Van Hoof (promotor), Prof. Georges Gielen (co-promotor)

## Carl D'heer

**THz and Sub-THz CMOS Electronics for High-Speed Telecommunication**

Promotor: Prof. Patrick Reynaert

## Tim Thielemans

**Fully Integrated Switched Capacitor Converters towards High Density Capacitive Energy Storage**

Promotor: Prof. Filip Tavernier

## Rohith Acharya

**Characterization and Modelling of the Quantum-Classical Interface for Scalable Superconducting Quantum Computing**

Promotor: Prof. Francky Catthoor (promotor), Prof. Georges Gielen (co-promotor)

## Peishuo Li

**Microelectronics for Microbiology**

Promotor: Prof. Marian Verhelst

## Marko Bakula

**Scalable Technologies for High Bandwidth Neural Interfacing**

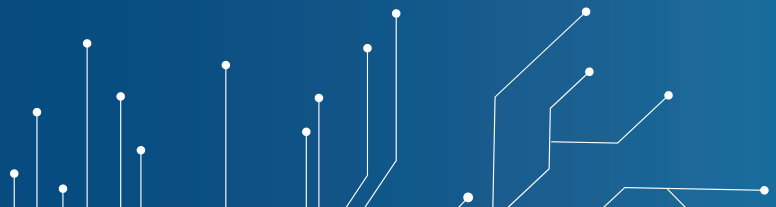
Promotor: Prof. Bob Puers (promotor), Prof. Michael Kraft (co-promotor)

## Nektar Xama

**Automated Design-for-Test and Data-Learning-based Methods for Testing of Analog and Mixed-Signal Integrated Circuits**

Promotor: Prof. Georges Gielen

# Awards



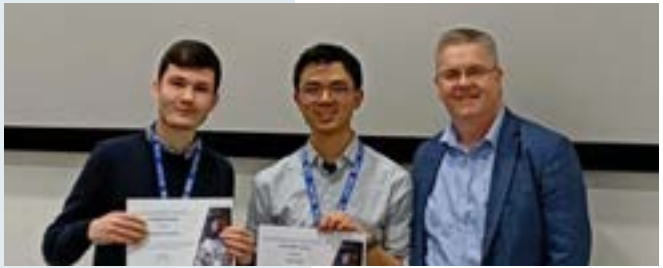
Ariane De Vroede and professor Patrick Reynaert won the 2023 Bell Labs Prize for their innovation of highly sensitive THz imaging using self-oscillating pixels. De Vroede is pictured here between Bell Labs Core Research President Peter Vetter (left) and Bell Labs Solutions Research President Thierry Klein.

Professor Michiel Steyaert received the 70th Anniversary Top ISSCC Contributors Award for his strong and sustained contributions to the International Solid-State Circuits Conference. He also became the Chair of the ESSERC steering committee. ESSERC is the new name of the merged ESSCIRC/ESSDERC conference, the most important devices and circuit design conference in Europe. The 50th edition will be organized in Bruges, Belgium, in September 2024.

Professor Marian Verhelst received the ERC Consolidator Grant for her research project BINGO, which officially started in May 2023. ERC Consolidator Grants are part of the EU's Horizon Europe program, and they help excellent scientists to pursue their most promising ideas. BINGO targets to outplay the hardware lottery for embedded AI.

Professor Georges Gielen has been elected as a new member to the Royal Flemish Academy of Belgium (KVAB), an autonomous scientific-cultural society that promotes scholarship, science and the arts. Its members develop science-based Position Papers and coordinate cycles of the Thinkers' Programme on grand societal questions, act as jury members in awarding prizes and organize presentations, colloquia, concerts and exhibitions.

# MICAS Awards



Jonah Van Assche and Jun Feng were awarded in the Analog Devices Student Design Contest for their work on analog-to-digital converters. Jonah won the 1st prize, while Jun ended 3rd.


The IEEE SSCS (Solid-State Circuits Society) Student Chapter Leuven received the 2022 Chapter with Best Education Program Award, in recognition of an outstanding record of consistent leadership and initiative in organizing activities that have contributed to the growth and vitality of the Solid-State Circuits Society. The Leuven Chapter is being run by MICAS researchers. In March 2023, they organized an event to celebrate the 75th anniversary of the transistor, with top local and international speakers, and an attendance of 140 people.

Bram Veraverbeke received the Analog Devices Outstanding Student Designer Award at the ISSCC2023 conference. Tuur Van Daele received the SSCS Predoctoral Achievement Award. Senne Gielen was awarded the 3rd prize in the Best Student Paper Competition at the RFIC2023 conference.

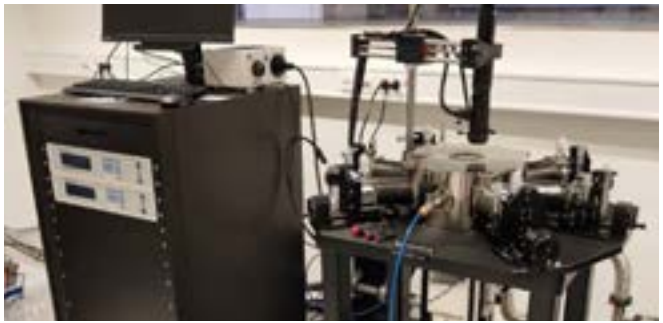
## MICAS Alumni & Friends Day

In 2023 we had two 'Micas Alumni and Friends' events. One during ISSCC in February in San Francisco and one in Leuven in November. Mingling up our alumni and our other friends twice this year proved to be a success. Lively debates about the future of semiconductors or more down to earth discussions about current and future cooperation naturally took place. Or even just catching up with an old colleague is always pleasant. At ISSCC the event was mainly a reception, as the conference already provided enough talks. In Leuven, we had two speakers: Bert Moons, a MICAS alumnus since 2018, talked about his career steps after his PhD and enlightened us about the future of AI at the edge as seen by Axelera AI, the company he co-founded. The second talk was held by our very own professor Michiel Steyaert. Spiced with some historical notes he showed us how MICAS, with its industry-driven academic research tradition, makes the difference in several research and application domains. When it comes to Michiel's own contributions, RF-CMOS is arguably the most prominent example. MICAS Alumni & Friends is an established event by now. Next edition at ISSCC 2024!

# Labs, services & equipment

Our state-of-the-art in-house measurement and technology labs are crucial assets to experimentally validate our research results. The equipment is also available to companies or other research groups in a service model.

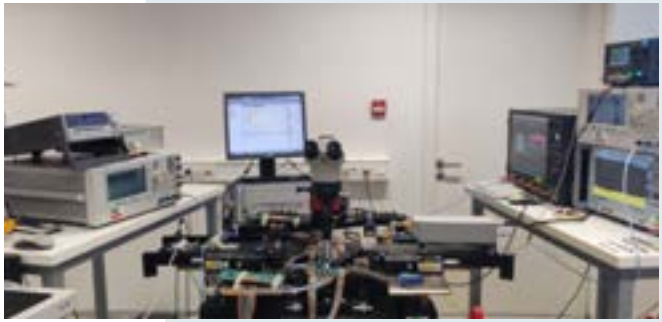
## IC-Lab LF: low-frequency measurement lab



IC-Lab LF contains specialized equipment in the range from DC to several GHz. The main focus of this lab is on low-noise, high-resolution signal generation and power source analysis.

Recently we have invested in a cryogenic station and cryogenic probe station, enabling us to perform electrical characterization at cryogenic temperatures down to 3.2 K.

## IC-Lab HF: broadband, optical, mm-wave and THz measurement lab



IC-Lab HF contains wideband measurement equipment such as signal analyzers, arbitrary waveform generators, oscilloscopes and vector network analyzers. An extensive set of high-performance instruments is available to ensure the best possible measurement accuracy up to frequencies well above 1 THz.

Thanks to the recently installed WR0.65 extenders, we can now generate and analyze signals up to 1.5 THz.

## Technology Lab: chip packaging and modification facilities

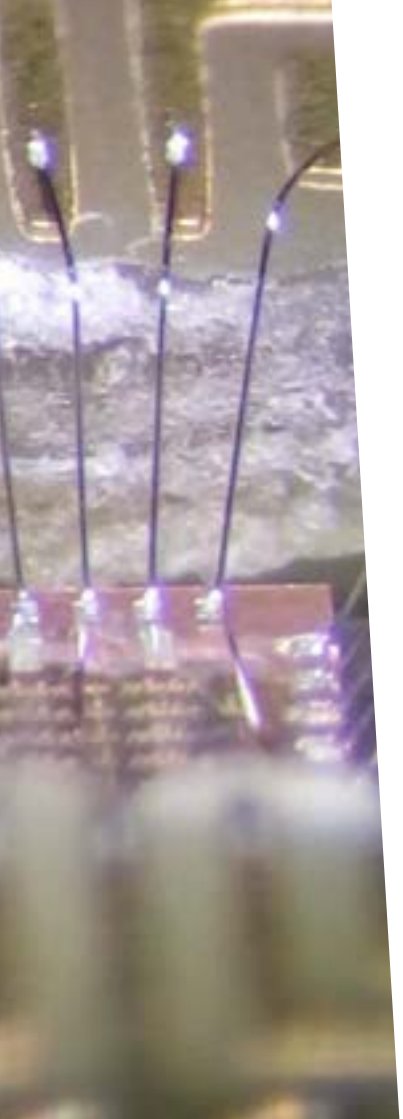
In the MICAS Technology Lab, we have all the necessary chip packaging equipment such as dicing, bonding, and flip-chipping tools. For advanced chip modification, a specialized Focused Ion Beam system (FIB) is available.

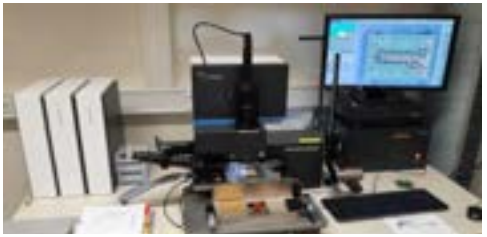
### Dicing & grinding

Our dicers can cut silicon wafers up to 300 mm in diameter and 0.8 mm in thickness. Glass wafers can be cut up to a thickness of 2 mm. We also cut dies that contain multiple designs into single chips. A specialized CNC-controlled grinding machine can perform decapsulation, silicon thinning and polishing of integrated circuits.

## Bonding

The bonding lab is specialised in packaging small series of a wide variety of state-of-the-art chip designs. Wirebonding can be done with both gold and aluminium wires, either on a PCB or in a package.





### Flip chip

With our Finetech Lambda FINEPLACER machines, we can flip chips with gold studs as well as with copper pillars and solder caps. If needed, we can place the gold studs ourselves with our gold bonding equipment. For chips with up to 40 connections we can use a thermosonic flip chip process at moderate temperatures (~100°C), while for higher amounts of connections we use a thermocompression process at higher pressures and temperatures (up to 300°C).

### Focused Ion Beam

For advanced chip modification, a specialized Focused Ion Beam (FIB) system is available. Several materials can be removed and deposited with nanometer accuracy so that circuits can be modified without the need for re-processing. A unique feature of the system is the increased working distance so that electrical components around the chip do not hinder the repair operation. This allows us to not only make modifications on single dies, but even on dies mounted onto a PCB.

BRUGES
9-12 SEPTEMBER
ESSERC 2024

# The Next Circuits for a Better Life

# MICAS ORGANIZES ESSERC 2024 IN BRUGES

Come and see the most recent innovations in solid-state electronics in Bruges, Belgium, as MICAS-KU Leuven collaborates with partners to co-organize the European Solid-State Electronic Research Conference (ESSERC) on September 9-12, 2024. The enchanting city of Bruges, with its UNESCO world heritage status, will be the stage for this exciting event, offering a unique blend of medieval charm and cutting-edge chip designs.

Led by General Chair Wim Dehaene and co-Chair Michiel Steyaert, ESSERC 2024 is a continuation of the past ESSDERC-ESSCIRC conferences, focusing on the presentation and discussion of recent advances in solid-state devices and circuits.

The 2024 edition will be the 50th in a row. Submit your own research paper by April 5, 2024, or join us as an attendee in Bruges to listen to top-notch plenary keynote presentations, interactive sessions, tutorials, and a glimpse into the future of solid-state circuits research, or to network with old and new friends in the world of chip design. Mark your calendars and stay tuned for updates at www.esserc2024.org — where history and innovation converge!

ESSERC 2024 website:

KU LEUVEN

micas
KU LEUVEN

Department of Electrical Engineering ESAT-MICAS,
Kasteelpark Arenberg 10, 3001 Leuven
www.esat.kuleuven.be/micas