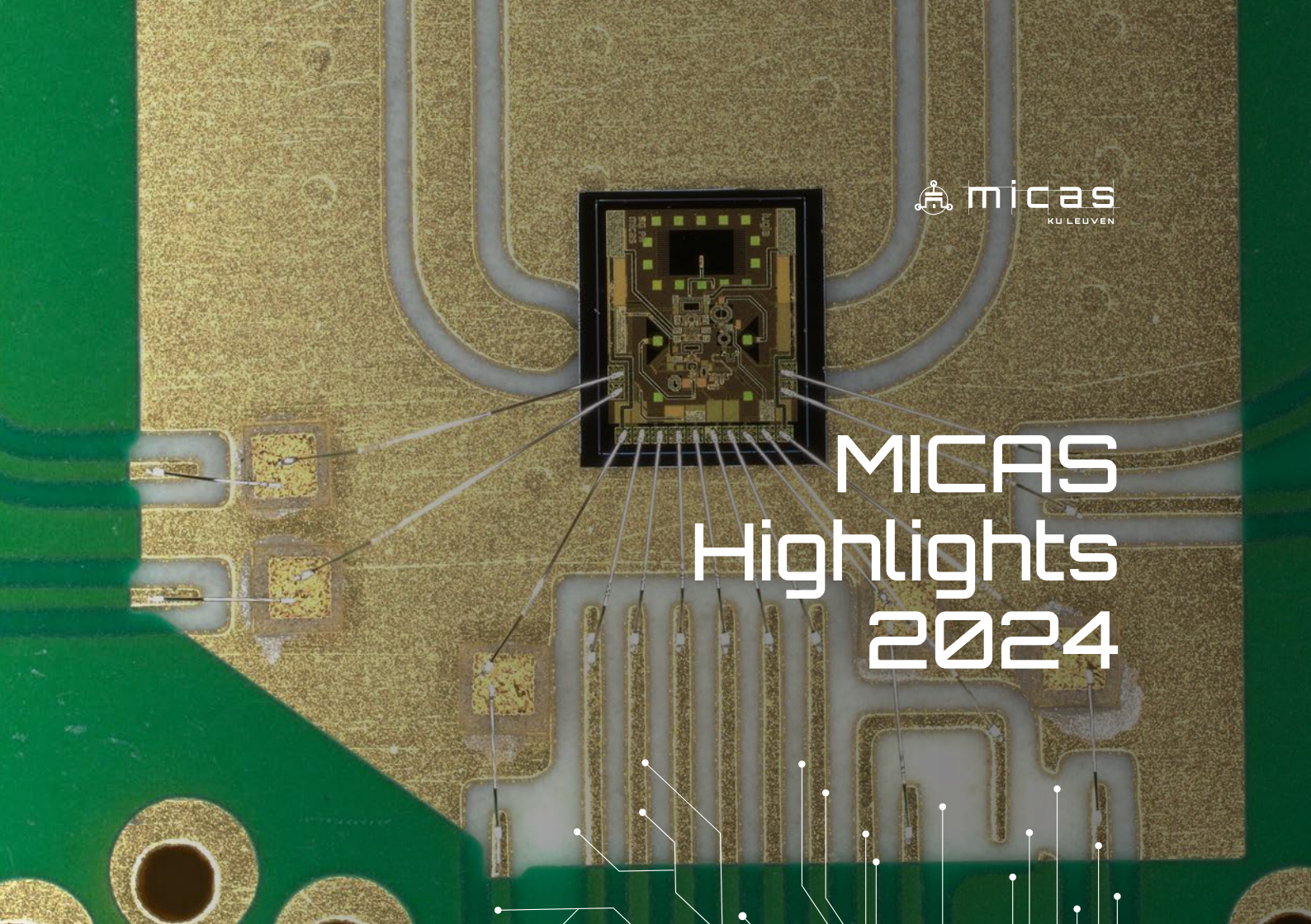

micas
KU LEUVEN
MICAS
Highlights
2024

Welcome to the MICAS Highlights 2024

a booklet that shines a spotlight on the past year's most remarkable achievements and advancements within our research division

What a year 2024 was for MICAS! A year of change and transitions. Transitions that close an era and transitions that ensure a bright future.

In April our founding father, Prof. Em. Willy Sansen sadly passed away. Willy was an international reference point for analog design. We will miss him, but we are also very grateful and proud to be his professional heirs.

In the fall of 2024, we switched professors. Michiel Steyaert retired after a career of more than 40 years at KU Leuven and Tim Piessens joined the group. And no, Tim is not the successor of Michiel Steyaert. It is simply impossible to replace a renowned RF and analog design authority like Michiel. Tim enriches the group with over 20 years of industrial analog IC design and his unique approach to that. This will make the MICAS circuits of the years to come even more outstanding.

Yet, in 2024 we also kept producing state-of-the-art advancing prototypes. Look at the revamped chip gallery on our website! We use technologies from 180 nm down to 12 nm. The first 7 nm designs are on their way. A big thank you to all our partners for providing the means for that!

2024 was also the year we organized the ESSERC conference in Bruges. Quite a job for the whole team, but it was worth it. The conference was a scientific success, participants loved historical Bruges and last but not least we had highly appreciated network events. It showed once more that even in a Zoom, Teams or skype world, nothing can replace in-person contacts.

So, looking back, 2024 may not have been a year of transition after all. MICAS is still MICAS: a bubbling stream of IC design creativity and innovative ideas. Dive into this highlights booklet to further convince yourself!

Wim Dehaene
On behalf of the MICAS staff
January 2025

Our mission

The three aspects of our mission are closely intertwined

RESEARCH

Through our research, we define and answer fundamental challenges in the field of chip design and generate breakthroughs that enable new solutions based on microelectronics, both in academia and in industry.

We push research to its technological limits, starting from visionary ideas, to developing them into silicon proven concepts that are picked up by the industry.

EDUCATE

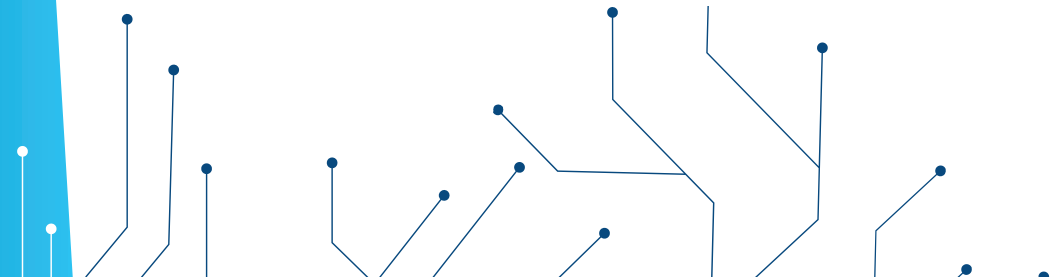
Rooted in our excellent research, we educate students to become leaders in electrical engineering and offer them the opportunity to further develop into PhDs.

Investing in our talented master and PhD students, by training them, by supervising them closely, sets them up to push the state of the art in circuit design.

INSPIRE

We want to make society aware of the role and importance of microelectronics and enthuse people to participate in this exciting field.

Building the next generation of circuits and sensors for a social, comfortable, healthy, safer and sustainable life.



Research

Through our research, we aim at defining and answering fundamental challenges in the field of chip design and generate breakthroughs that enable new solutions based on microelectronics.

MICAS pursues a wide range of fundamental to applied research across nine research domains, which cover different aspects of integrated circuit design:

Research approach

The MICAS research agenda spans a very wide range: from fundamental to applied research, from conceptual explorations to chip prototype realizations. As such, a research project at MICAS typically goes through the following sequence of steps:

- Investigation of an innovative concept towards an implementable architecture;
- Design and fabrication of a demonstrator chip to validate the research results;
- Characterization of the chip in our in-house measurement labs;
- Analysis of the results as a starting point for a next design cycle.

This sequence is then repeated such that the initial concept can gradually mature into research results that can be transferred to industry and society. The many projects in the MICAS research pipeline are funded through various channels: from internal KU Leuven and basic science funding, over Flemish and European funding, often in collaboration with industry, to bilateral industrial funding. The Intellectual Property arrangement is tailored towards the specific type of collaboration, meeting the exclusivity requirements of our partners without blocking our own academic freedom and research roadmap. In addition to our research on chip innovations, we also investigate and develop computer tools and methodologies to more efficiently design and test chips, and we work on innovative algorithms and modeling methods to address problems not (yet) covered by commercial tools. More information can be found on the Research Domain pages.

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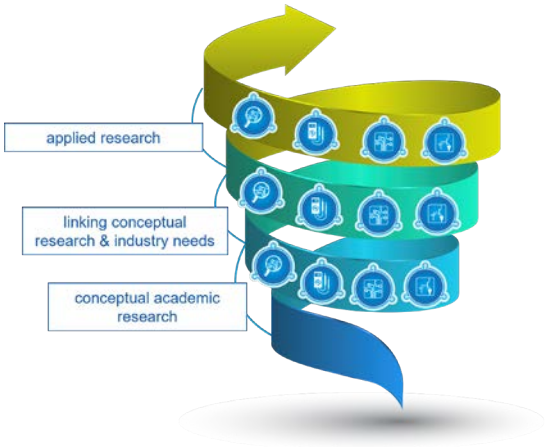


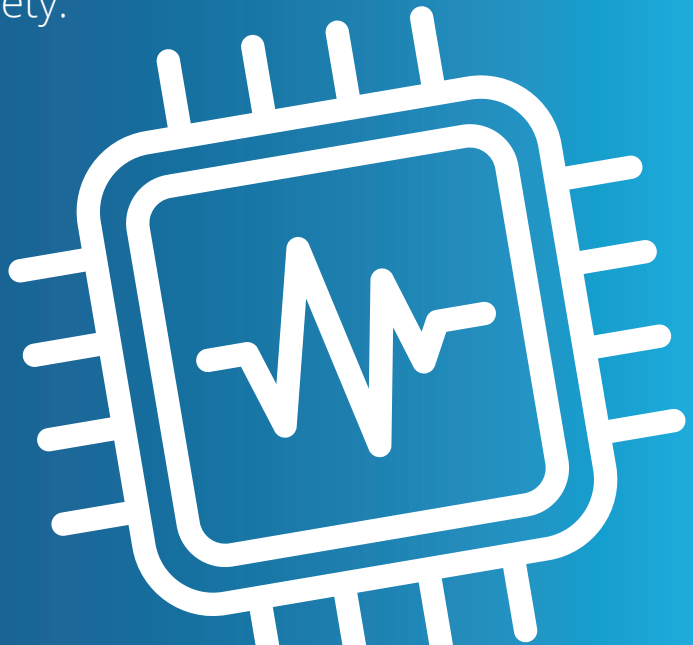
Learn more about some of our projects on our website.

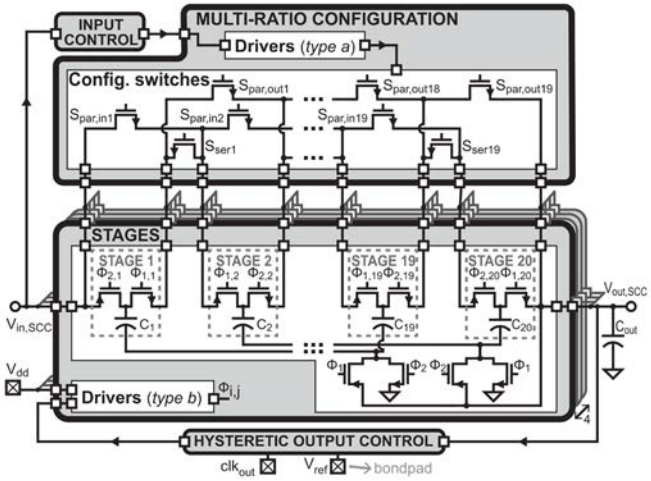
Analog and power management circuits

"Analog and power management circuits remain vital components in our highly digitized society."

Analog circuits remain vital components in our highly digitized society. Analog circuits span various challenges and applications, ranging from analog front ends, amplifiers, filters, etc. Scaled CMOS technologies, with their reduced supply voltage and intrinsic gain, challenge such building blocks fundamentally.

Additionally, more advanced power management circuits are emerging as power efficiency is critical to increasing battery life and enabling ever more powerful applications. The trend towards higher voltages, higher power densities, higher conversion ratios, and a higher integration level remains relevant. MICAS is a strong player in all these domains. We focus on innovative approaches and on the use of standard CMOS and more innovative integration technologies.



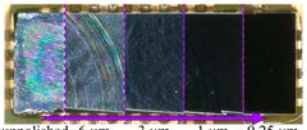


2024 highlights on analog and power management circuits

A single-chip high-voltage AC-DC and DC-DC converter

We have implemented and successfully tested a fully integrated 230 V_{rms}-to-12 V_{dc} AC-DC converter in a 180 nm high-voltage CMOS SOI technology. The primary block is a switched-capacitor DC-DC converter, which is reconfigured by parallelizing stages using low-voltage configuration switches. These configuration switches are connected between internally generated DC nodes that do not swing at the switching frequency, thereby avoiding the periodic charging of the corresponding drain capacitances. An efficient pre-charging technique enables to use this converter as an AC-DC converter without breaking down its low-voltage components. Additionally, a linear regulator is incorporated into the converter, resulting in a 2× smaller capacitance to buffer the AC zero crossing. The chip also features compact drivers and an efficient resettable capacitive voltage divider for input sensing. The measured power density is 9 mW/mm² at 55.1% efficiency, advancing the power density of fully integrated state-of-the-art AC-DC converters by >5000×.

This work was published in the IEEE Journal of Solid-State Circuits with DOI: 10.1109/JSSC.2023.3340976.



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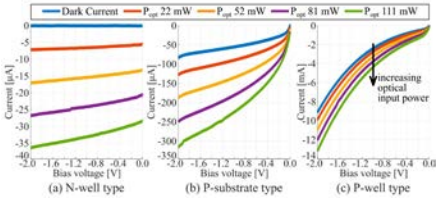
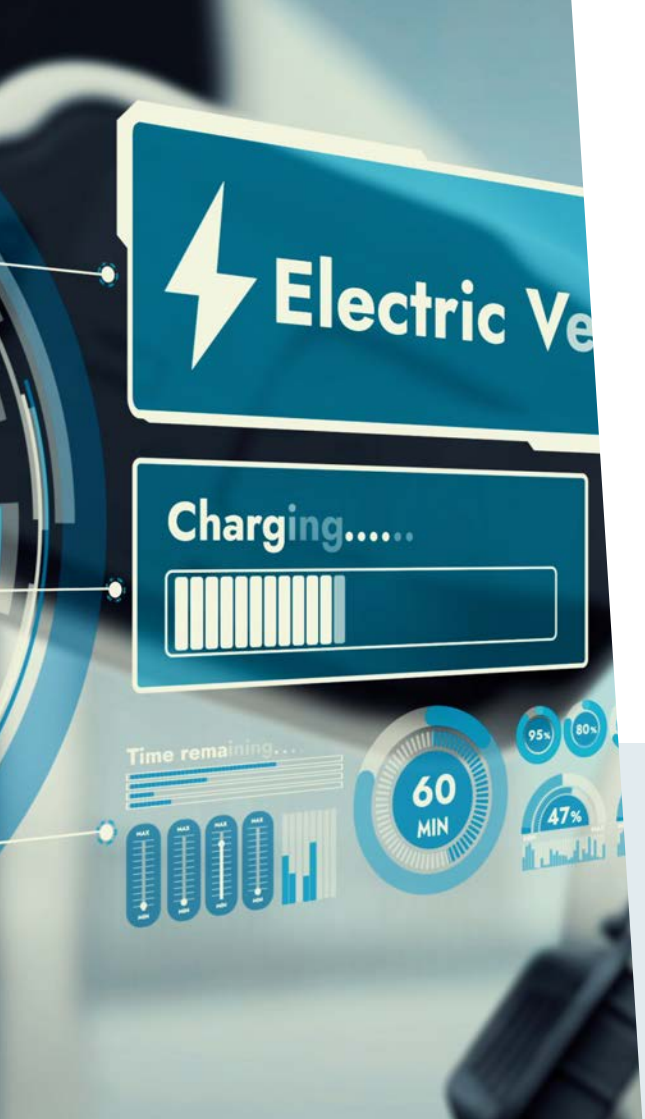


Characterization and modeling of Schottky photodiodes in 65 nm CMOS

CMOS remains the dominant technology to integrate a growing number of electronic systems. However, what has always deemed impossible was to detect photons as silicon is transparent for the traditional telecommunication wavelengths of 1340 nm and 1550 nm. Therefore, silicon photodiodes cannot detect such photons. However, Schottky photodiodes in CMOS can convert such photons, albeit with limited responsivity. Low-noise readout circuits can alleviate this challenge so that fully integrated optical receivers become a reality at the telecommunication wavelengths.

We have implemented, characterized, and modeled a variety of CMOS Schottky photodiodes with the aim to understand the intrinsic behavior of such devices. Moreover, we have done extensive temperature sweeps to better understand the mechanisms. The conclusions of this work have been presented at the 2024 IEEE Photonics Conference.



Contact

Analog and power management circuits

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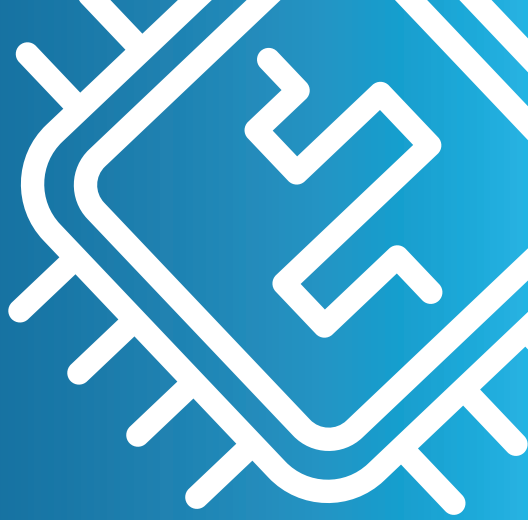
"Analog and power management circuits remain at the core of our research even as technology scales and our world becomes more digital."

Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

Mixed-signal circuits and data converters

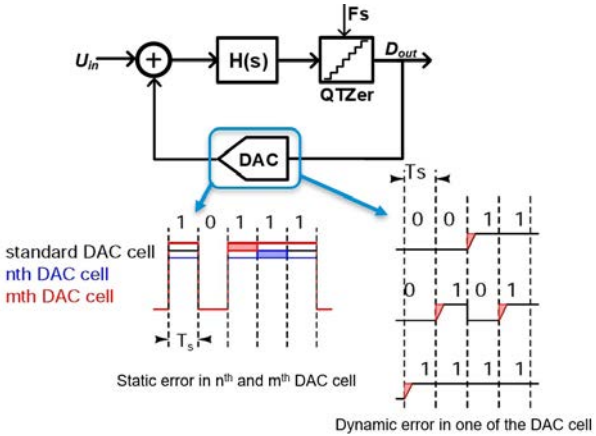


"Data converters interfacing the analog and digital realms are among the most critical components of most modern electronic applications."

Data converters interfacing the analog and digital signal realms remain among the most critical components of many modern electronic applications. The need to faithfully preserve the signal information across domains continues to pressure data converters to deliver an ever-higher bandwidth and linearity while reducing the power consumption.

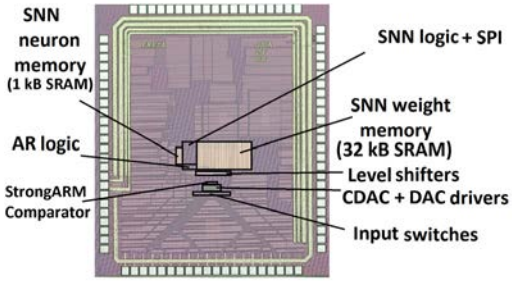
Exciting new architectures and circuits are continuously being introduced that push data converters towards these ever-higher performances. MICAS has always been a renowned contributor in this domain. This trend continues as we work on various innovative architectures and circuit building blocks, focusing on low latency, high input bandwidth and increased energy efficiency for edge and sensing as well as telecom applications.

2024 highlights on mixed-signal circuits and data converters



Energy-efficient wide-bandwidth continuous-time ΔΣ ADCs

The insatiable need for ever-increasing data communications demands transceiver circuits with ever-wider bandwidths. Continuous-time Delta-Sigma (CT-ΔΣ) ADCs exhibit system-level power advantages in wireless communication systems. With increasing channel bandwidths (200 MHz and above) and reducing oversampling ratios, however, the power consumption and the nonlinearity of the main feedback DAC become primary performance limitations. Therefore, to achieve these wider bandwidths at high energy efficiency, a new Gm-C based loop filter structure is being explored in combination with a foreground digital calibration method for both dynamic and static errors of the main feedback DAC. The chip prototype in 16 nm CMOS is currently being measured.



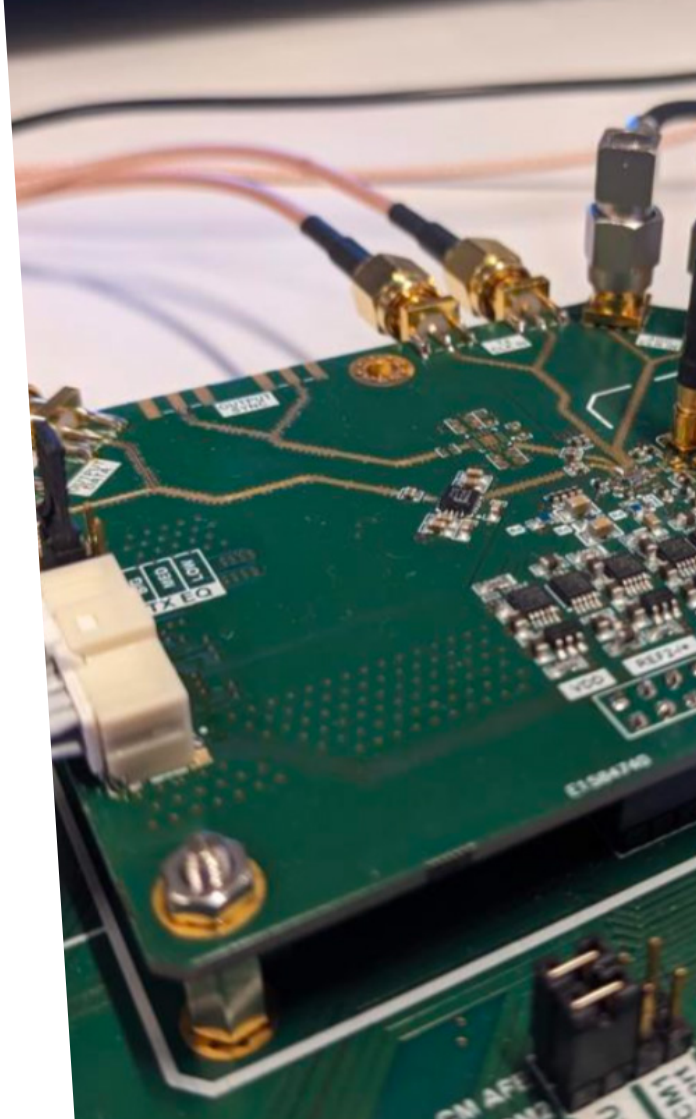
Neuromorphic, event-driven level-crossing ADC with high power efficiency

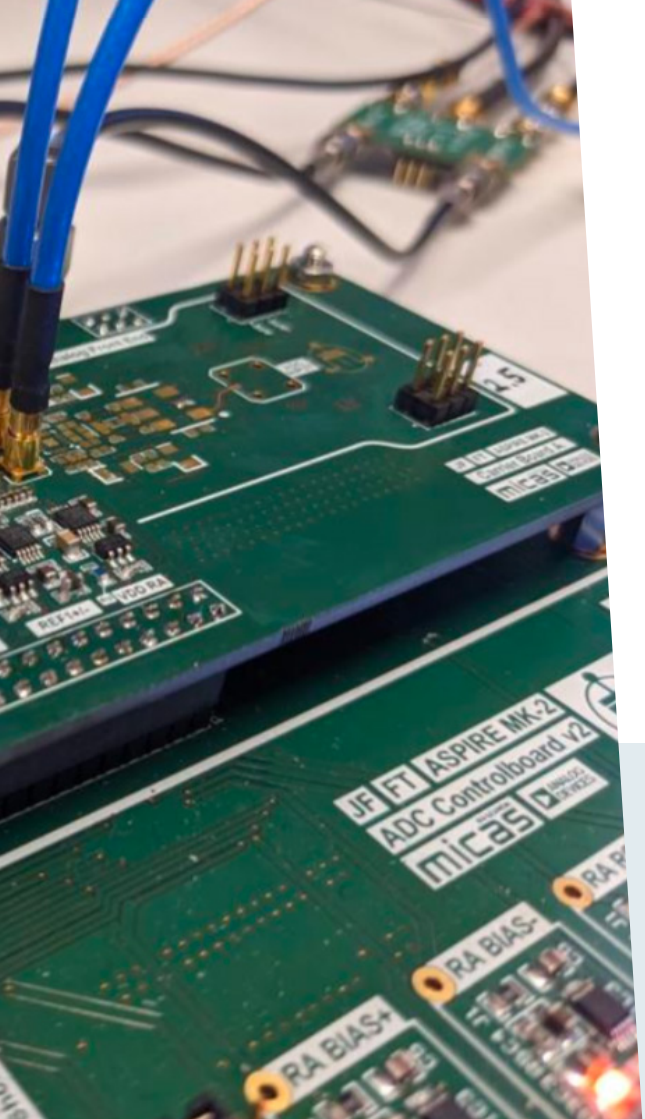
Level-crossing ADCs are neuromorphic, event-driven data converters that are suited for resource-constrained applications where intelligent sensing must be provided at tight energy and area budgets, such as in edge devices or biomedical implants.For time-sparse signals such as ECGs, neural action potentials, etc., such converters can result in significant reductions in data bandwidth, chip area and energy consumption compared to conventional ADCs. Their event-driven nature makes them also ideal to generate spiking signals as inputs to spiking neural networks (SNNs). To validate this, the FREYA chip has been developed. FREYA is an 8-channel event-driven SoC for end-to-end sensing of time-sparse biosignals. The 8 multiplexed channels are read out through a fully programmable level-crossing sampling analog-to-spike converter that encodes the analog input signals into input spikes for the on-chip SNN processor. The prototype IC in 40 nm CMOS has an active per-channel area of only 0.023 mm2, a 7x improvement over the state of the art, with a power of 20.8 µW per channel. The results have been published in the IEEE Transactions on Biomedical Circuits and Systems.

A novel high-speed precision ADC for low-latency applications

Latency is an increasingly critical specification in modern applications. This holds true for electrical and optical ADC-based transceiver links, and for high-precision applications, such as digital control loops for high-performance power management, or audio and radar for automotive. Any application with a short round-trip delay or a fast feedback loop requires a low-latency ADC. However, latency has traditionally been sacrificed for other ADC performance metrics.

We have developed a 200 MS/s 14-bit two-stage ADC using asynchronous pipelining with the aim to obtain a constant and low latency of only 8 ns regardless of the sample rate, which is much lower than published and commercially available ADCs with similar speed and resolution specifications.





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Mixed-signal circuits and data converters

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"Seamlessly bridging the analog-digital divide for a broad range of applications is at the forefront of our research."

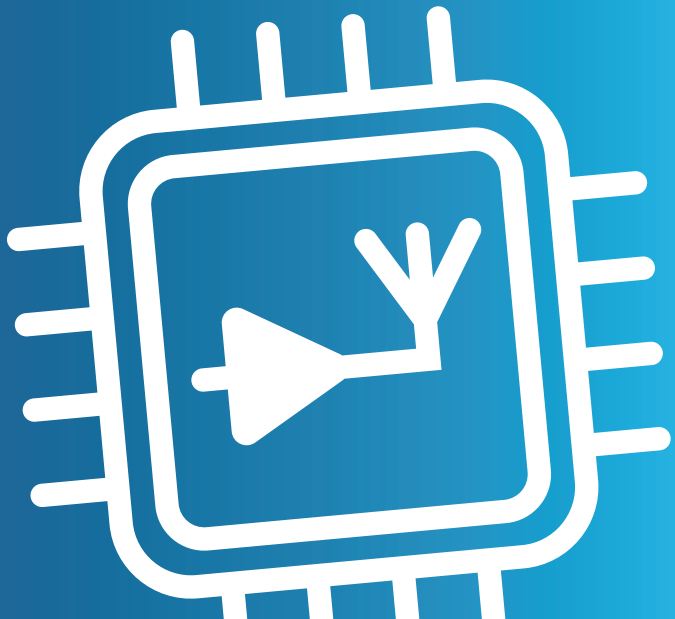
Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

RF, mm-wave and THz circuits

"MICAS has a long tradition in the broad field of RF circuits."

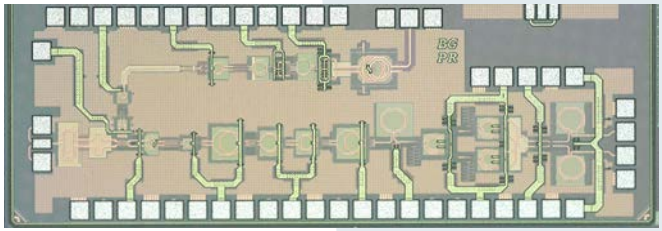
MICAS has a long tradition in the field of RF circuits in general. Whether it is for cellular 5G communication, unlicensed applications, radar, sensing, imaging or future 6G communication, the research in this field is continuing with a wide range of topics. As operating frequencies and -more importantly- bandwidths go up, novel architectures and circuit techniques are needed. Furthermore, the research on RF, mm-wave and THz circuits is also diversifying with respect to semiconductor technologies. Whereas a strong focus on standard CMOS has been the mantra of MICAS in the past, today a wide range of technologies, such as GaN, GaAs, InP, FDSOI and FinFET are being used in our research projects for future communication, ranging and sensing applications. This allows us to focus on the best technology for each specific application.

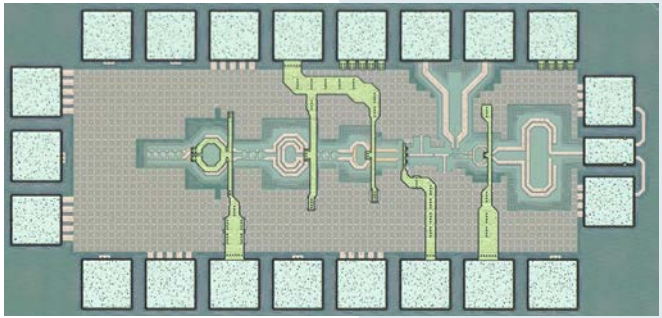


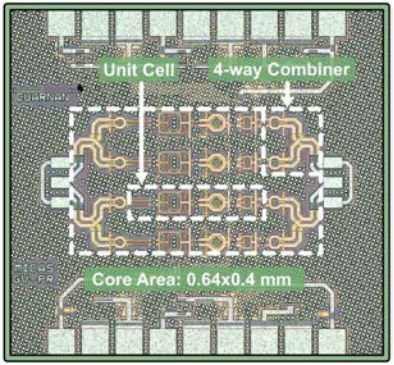
2024 highlights on RF, mm-wave and THz circuits

J-band in 16nm Finfet

A J-band (252-325GHz) TX and RX chip set for near-field communication, implemented in 16nm FinFET CMOS was implemented and measured. Both systems are designed to utilize amplitude-shift-keying (ASK) modulation and to operate non-coherently, alleviating the need for a synchronized LO between TX and RX. Both chips are characterized standalone in a probe station. The TX achieves an output power of -19dBm at 270GHz center frequency with a 3-dB bandwidth of 45GHz. The RX has a conversion gain of 31dB with a baseband bandwidth of 0-25GHz. The performance of the RX is verified with modulated measurements, with up to 20Gbps NRZ at 280GHz carrier, limited by the measurement setup. The chips were presented at RFIC 2024.







D-band PA with low AM-PM distortion

A high-linearity and high-backoff-efficiency power amplifier (PA) for D-band (110-170 GHz) communication in 22 nm CMOS FD-SOI technology was developed and measured. Fully differential eight-way power combining with extremely low insertion loss is implemented, enhancing the common-mode-rejection-ratio (CMRR), output power and linearity with bypass capacitors placement and sizing. Cascading moderate and deep class AB stages, together with a careful choice of the value of common-mode stability resistors, further improves the amplifier's linearity. The small-signal gain and bandwidth (BW) are 16 dB and 21 GHz. The OP1dB and P_{sat} are 11.4 dBm and 14.6 dBm while maximum PAE and 6dB backoff PAE are 10.6% and 2.8% respectively. The highest demonstrated data rate is 32 Gb/s, using a 16-QAM modulation scheme at an average output power and PAE of 8.1 dBm and 4.2% respectively. This work was presented at RFIC 2024.

Contact

RF, mm-wave and THz circuits

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"As operating frequencies and bandwidths go up, novel architectures and circuit techniques are needed."

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Wireline and optical circuits

"Answering the never-ending need for energy efficiency, higher speeds, and lower latency."

The research on wireline and optical circuits at MICAS is pushed by the never-ending need for energy efficiency, higher speeds, and lower latency. But at the same time, MICAS also explores innovative communication concepts such as full-silicon optical solutions enabling 1310/1550 nm communication and polymer microwave fibers (PMF).

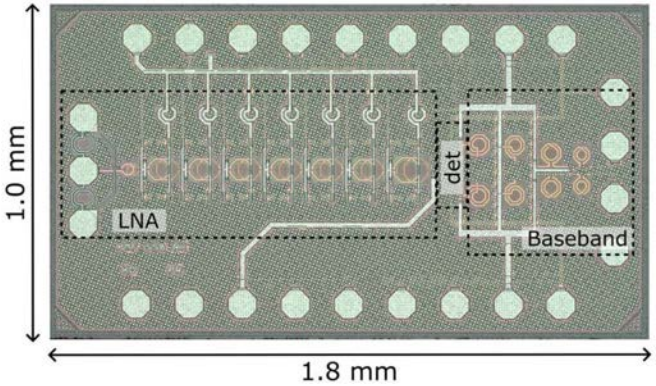
Optical interaction is highly challenging in silicon. The high doping concentrations and low supply voltages of CMOS result in small and slow responses of photodiodes. Moreover, 1310/1550 nm light is not absorbed due to the high bandgap. However, the trend towards higher integration levels can also be seen in this challenging domain thanks to innovative circuit techniques combined with novel conversion mechanisms between the optical and electrical domains. MICAS has been a trendsetter in this domain for many years.

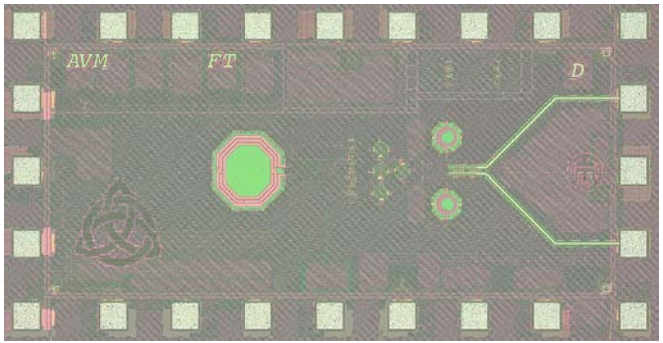
Also, concerning polymer microwave fibers, MICAS stays in the leading position by pushing the data rate and distance boundaries. Not only is the research investigating silicon integrated front ends for PMF, but also couplers, duplexers, and fibers are being investigated to obtain the optimal solution for a wide range of connectivity applications.

2024 highlights on wireline and optical circuits

Receivers for Polymer Microwave Fibers

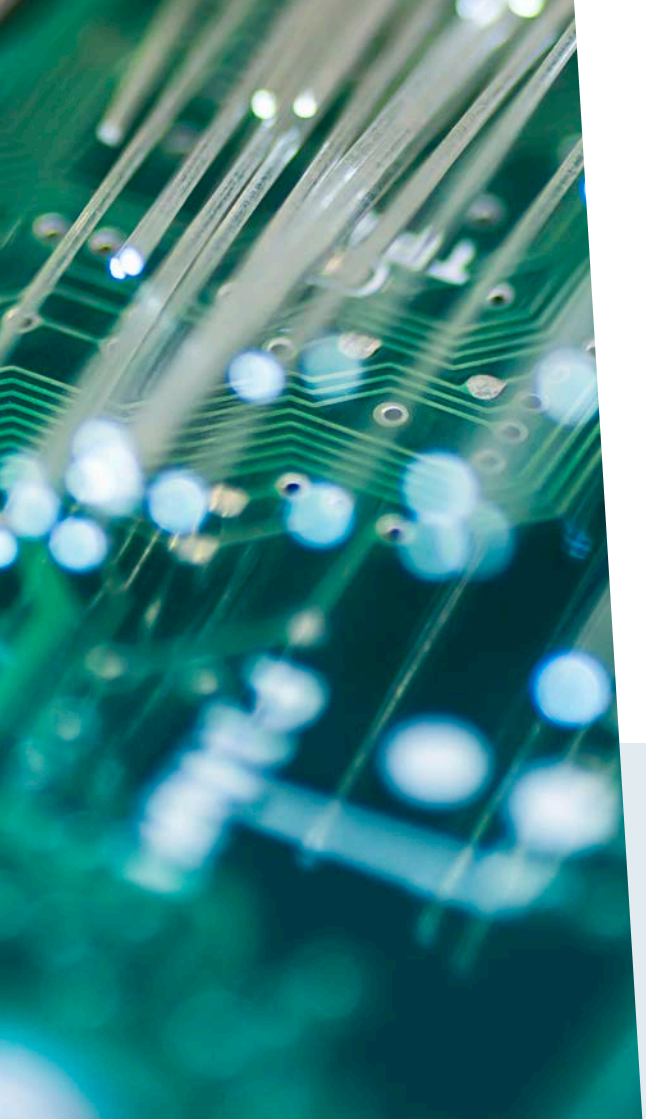
A non-coherent receiver design for dielectric waveguide communication was implemented in 22 nm FD-SOI. Envelope-detectable single-sideband modulation is employed to improve the spectral efficiency and to avoid carrier recovery. Data rates up to 36 Gb/s are shown over a 1−m fiber and up to 32 Gb/s is still obtained at 5 m. These high symbol rates are achieved without any equalization, leading to low-latency and low-power wireline communication competing with copper and optical. This work was presented at ESSERC 2024





Optical injection-locked oscillators for optical clock receivers

This research aims at fully integrating a 1310 nm optical injection-locked oscillator based on Schottky photodiodes in a standard 65 nm CMOS process. The aim is to facilitate the opto-electrical integration in clock transmission, recovery, and synchronization for long-distance communication systems. This work uses an on-chip Schottky photodiode to detect the received optical clock signal and convert it into a small photocurrent that is used to lock an LC-oscillator. This work was presented at ESSERC 2024.



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Wireline and Optical circuits

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"MICAS has a leading role in the field of Polymer Microwave Fibers, by pushing the boundaries of both data rate and distance."

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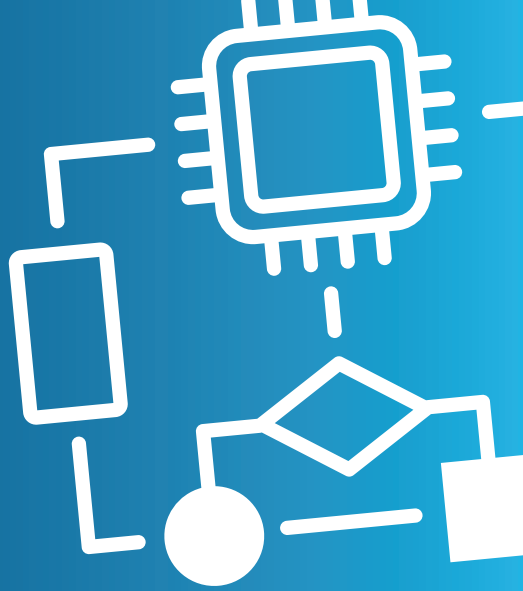
Computer-aided hardware design and test



"MICAS performs research on innovative CAD algorithms, modeling methods and design methodologies."

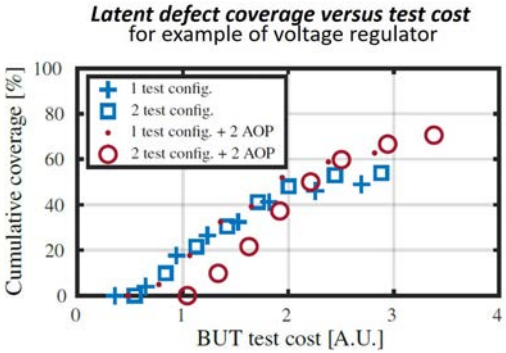
The design of electronic integrated circuits requires computer-aided design (CAD) tools for simulation, design and test. For many decades, MICAS is carrying out research on groundbreaking innovative algorithms, modeling methods and design methodologies to address emerging problems not (yet) covered by commercial EDA tools. These include the accurate modeling and efficient simulation of emerging phenomena in advanced CMOS as well as beyond-CMOS technologies, such as the stochastic modeling of time-dependent aging phenomena in deeply scaled CMOS, or the modeling of emerging quantum devices and circuits.

In addition, pioneering methods for the design and layout optimization and automated synthesis of analog, mixed-signal and RF circuits remain a major focus point of the MICAS research. Disruptive techniques from machine learning and AI are being explored to increase the capabilities for the automated synthesis and verification of integrated circuits. Finally, MICAS explores novel algorithms and design-for-test techniques to boost the effectiveness of analog/mixed-signal test programs and to automatically generate test programs with a higher test coverage in a shorter time, both for hard as well as latent defects.

2024 highlights on computer-aided hardware design and test

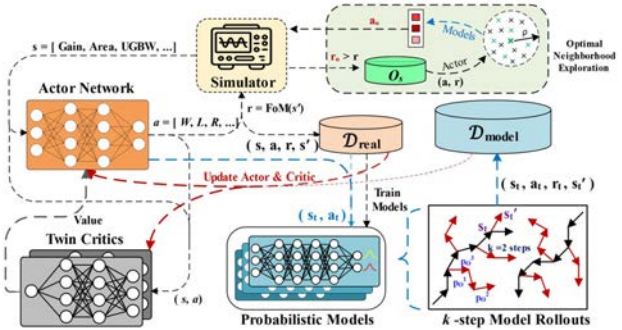
ERC project AnalogCreate: AI/machine learning methods for analog/mixed-signal integrated circuit synthesis and test

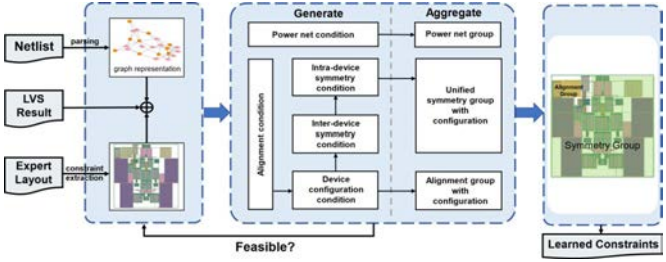
Prof. Gielen's AnalogCreate ERC project is up to full speed. Despite the progress in CAD methods over the past decades, the design and test of analog/mixed-signal ICs in industry still largely occurs manually by designers, resulting in long and error-prone design and test development times. Supported by the ERC Advanced Grant AnalogCreate, a large research effort is taking place at MICAS to develop sophisticated algorithms based on techniques from machine learning and artificial intelligence, in combination with advanced optimization and stochastic methods. The goals are the more efficient automated design and layout synthesis of analog/mixed-signal ICs, the structural synthesis of novel circuit topologies, as well as the more effective automated verification of analog circuit designs. Key is the self-learning of constraints from example designs and layouts created by experts. Also, novel test methods are being explored using machine learning techniques to boost test coverage. First conference publications have been made in the past year, with journal papers on the way.



Methods and models for improved detection of latent defects in analog/mixed-signal ICs

Safety-critical applications like automotive require test escape rates well below the 10-ppb level for their integrated circuits. For a decade now, MICAS has been working towards this goal, exploring new test metrics, proper fault models, novel design-for-test methods and circuits, innovative test analysis methods, pioneering test generation algorithms, etc. With these improvements being transferred towards industrial practice, the biggest challenges currently being addressed are the increased coverage of latent defects as well as reducing the long lead time for analog test program development. By innovatively applying machine-learning-based classification to the outputs of industrial test programs, highly increased latent defect detection rates have been obtained beyond 95%. The latest research in this area focuses on further boosting the coverage using analog blocks with continuous BIST monitoring.





Efficient machine-learning-based circuit and layout synthesis of analog integrated circuits

Innovative machine-learning-based methods have been developed to optimize the sizing and layout of analog integrated circuits. A Model-Based Policy Optimization (MBPO) method has been developed to boost the sample efficiency of reinforcement learning for analog circuit sizing. It leverages an ensemble of probabilistic dynamic models to generate short rollouts branched from real data for a fast but extensive exploration of the design space. This model-based MBTD3 approach has been validated on analog circuits of different complexity, such as a data receiver. This work has been presented at the DAC 2024 conference.

Making good use of human designer heuristics as constraints that steer today's tools is key to balancing efficiency and design space exploration. A flexible generate-and-aggregate framework has been developed that can self-learn various layout constraints, such as alignment, symmetry, and device matching, from some expert-generated example layouts. Through feature matching, the learned knowledge can then be transferred as constraints for the layout synthesis of different circuit topologies. This work has been presented at the DATE 2024 conference.

Testing and modeling of quantum qubits: matching the behavior at room and cryogenic temperatures

Quantum computers aim at solving computationally hard tasks exponentially faster than classical computers. Today's qubits, however, operate at cryogenic temperatures. Testing the correct functioning of the qubits at such temperatures, however, is extremely expensive in time and cost, not only due to the required equipment and the long cool-down time, but also due to the limited number of packaged devices that can be tested in a single cool-down cycle. Therefore, MICAS and imec are carrying out research to find test routines for high-volume room-temperature screening of spin qubit arrays, by searching for device metrics that are measurable at room temperature (or just below) and that serve as good predictor for the qubit's performance at cryogenic temperatures. This work has been presented in IEEE Electron Device Letters. In addition, a hybrid Hamiltonian approach has been developed to efficiently simulate quantum qubit circuits, and analyze for instance the impact of noise on qubit stability. This work has been published in the IEEE Transactions on Quantum Engineering.

Contact

Computer-aided hardware design and test

Prof. G. Gielen
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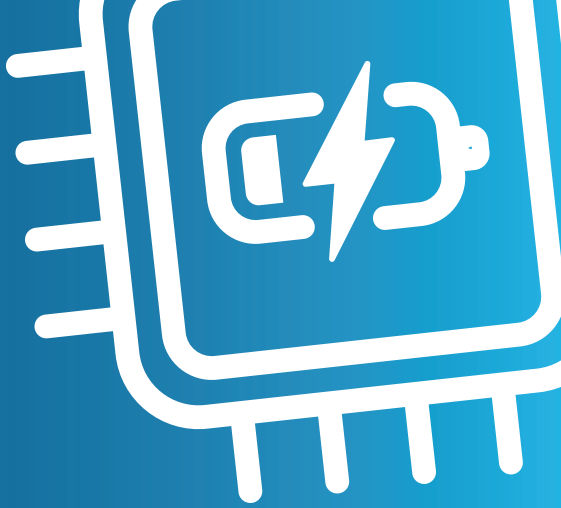
"The goals are the automated design and layout synthesis of analog/mixed-signal ICs, the creation of novel circuit structures, as well as a more effective automated verification and test generation for analog circuits."

Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

Ultra-low-power digital SoCs and memories

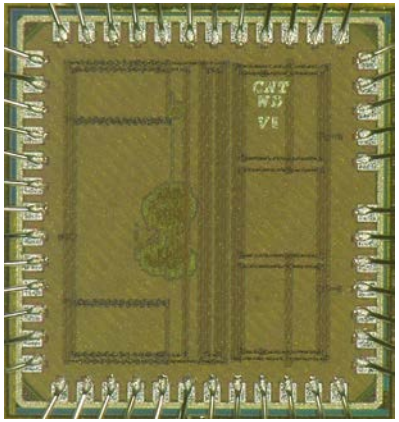


“Exploring new digital design techniques and architectures to increase energy efficiency in digital processors”

Further evolution of applications in robotics, autonomous vehicles or biomedical wearables rely on ultra-low energy consumption of the electronics circuits they encompass, while also requiring a large degree of flexibility and programmability. The deep-submicron evolution of silicon technology does not favor low-energy design, due to the ever-increasing leakage and technological variability on the one hand, and the system complexity on the other hand.

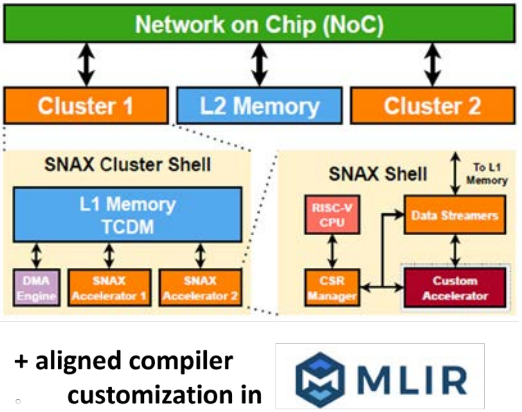
We reached the point where the classical remedies, e.g. multi-VT libraries or margined corner-based design, no longer suffice. In 2024 MICAS continued to explore new digital design techniques and architectures to increase the energy efficiency in digital circuits, ranging all the way from low power memories to flexible customized compute fabrics.

2024 highlights on ultra-low-power digital SOCs and memories



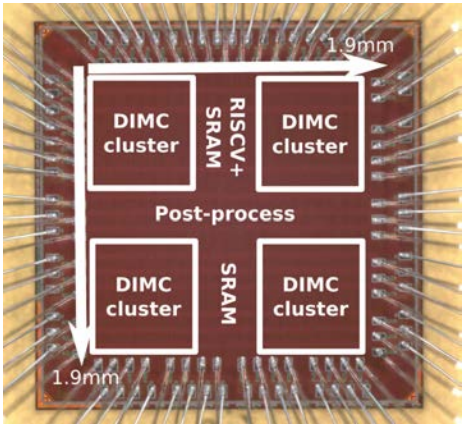
In-situ timing monitoring for ultra-low-voltage, energy-efficient RISC-V cores.

Our long-running research effort on in-situ timing monitoring produced another highlight this year. We further refined our detection techniques with transition detectors that are triggered before the clock cycle is completed, e.g. at 75% of the clock period. We baptized this technique Early Monitoring Error Prediction (EMEP). This simplifies the detection and reduces the risk on undetected activity. To prove the EMEP technique and benchmark it versus our previous work based on endpoint timing detection, we implemented the new technique in a RISC-V core. We can save up to 40% on energy compared to a fully margined design, with only 12.5% energy margin left. This was published in ESSERC2024. A journal paper elaborating on EMEP is on its way.



Flexible RISC-V-based multi-accelerator fabrics with SNAX

A scalable heterogeneous multi-accelerator architecture enables high efficiency and flexibility for diverse signal processing workloads, but requires tight integration between accelerators and memory without sacrificing scalability. To address this, MICAS developed an open-source framework for smooth accelerator integration, denoted SNAX. SNAX consists first of all of a standardized hardware template for accelerator integration, featuring a lightweight management core, tightly coupled memory with streaming ports and a smart DMA for data layout transformations. This architecture template is paired with an MLIR-based compilation framework, which allows to quickly customize the compiler to a specific accelerator combination. Together, these frameworks aim to maximize accelerator efficiency, while minimizing integration efforts towards heterogeneous scalable multi-accelerator systems. The first SNAX-enabled tape-out will be happening in 2025!



Digital in-memory computing for vision recognition on the edge

DIMC was already on the map when we showed an optimized in memory compute macro. 2024 brought us much further. We were able to tape out 'HUNBN', a 16 nm FinFET chip demonstrating a complete IMC based accelerator. It shows that DIMC is an energy-friendly alternative for classic accelerators, especially when the model is moderately sized and can fit at once on the chip. This gave us a U-net/CNN chip with a best efficiency of 24 TOPS/W (4b, 30 frames/s). HUNBN was published in ESSERC 2024 and was selected for publication in the Journal of Solid-State Circuits special issue on ESSERC 2024.

Contact

Ultra-low power digital SoCs and memories

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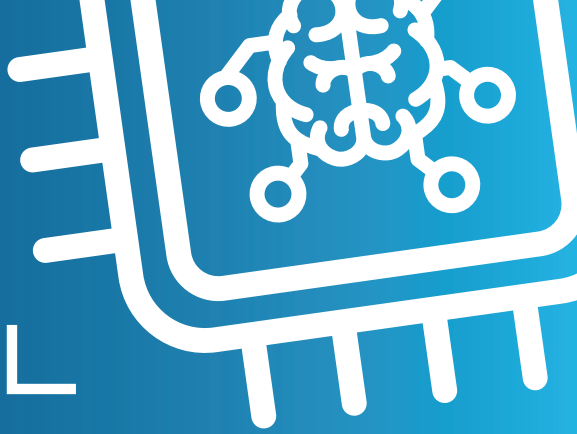
"The introduction of AI techniques makes the power consumption challenge in IoT applications even bigger. The advanced logic and memory designs of MICAS will help to solve this challenge and unblock the road to a smarter, safer and more sustainable society."

Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

Hardware-efficient AI and ML

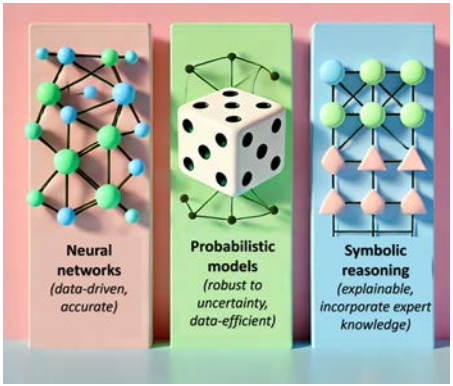


"Meeting the growing demands of diverse AI workloads requires fundamentally new hardware architectures that balance customization and flexibility, together with aligned scheduling and compilation frameworks."

Machine learning and artificial intelligence (AI) solutions are increasingly pervasive in modern society. Cloud-based smart AI assistants are revolutionizing the way we work, learn, and communicate. At the same time, advances in AI and signal processing at the edge are unlocking unprecedented capabilities in robotics, smart appliances, autonomous vehicles, and wearable devices. However, over the past decade the energy and carbon footprints of these workloads have grown at an extraordinary pace, surpassing even Moore's law.

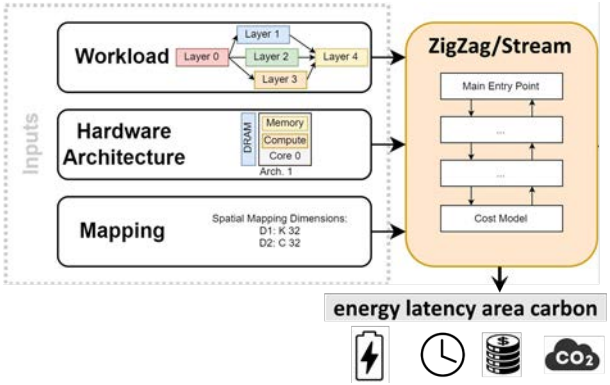
Fundamental circuit and architecture research is required to sustain AI's transformative impact. Also in 2024, the MICAS team has continued to address these challenges by exploring improved hardware architectures, advanced chip implementations, and hardware-algorithm co-optimization techniques for hardware-efficient AI and edge solutions.

2024 highlights on hardware-efficient AI and ML



AI = neuro + probabilistic + symbolic!

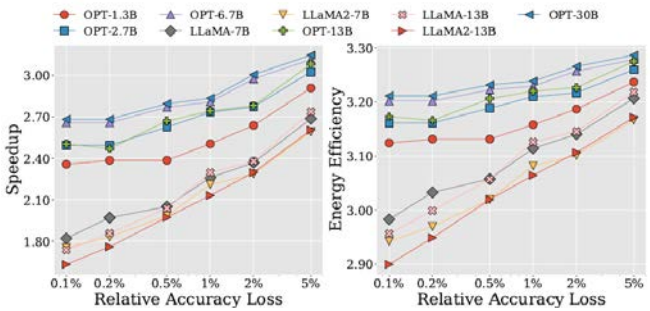
As AI evolves, future systems will require a broader variety of models beyond neural networks to achieve reliability, efficiency, and transparency. Neural networks excel at processing complex data, yet are increasingly combined with probabilistic models and symbolic reasoning because of the improved robustness and explainability. However, current CPU, GPU or TPU hardware architectures struggle to support these diverse workloads effectively. In 2024, we started building the heterogeneous hardware platforms required to support these diverse workloads, consisting of multiple co-operative AI accelerators. Next to more flexible GeMM accelerators, an accelerator for hyper-dimensional computing and an Ising processor, this also includes our AIA accelerator for probabilistic model inference, presented at ESSCIRC 2024.



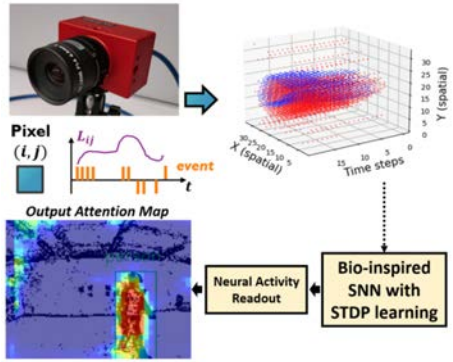
ZigZag / Stream design space exploration frameworks

Expanding ZigZag and Stream towards LLM support, carbon estimations and sparsity modeling

Since many years, the MICAS team has been developing the ZigZag and Stream design space exploration tools, which are capable of optimizing AI hardware accelerator architectures as well as workload execution schedules. In 2024, these tools received an update of their user interface, and have been expanded in several directions: ZigZag-LLM provides an extension for exploration and scheduling of the emerging Large Language Model (LLM) workloads. Additionally, ZigZag has been equipped with a carbon model, to not only be able to consider the latency, energy and area consequences of particular design choices, but also the total carbon cost. Finally, a stochastic framework has been developed, which allows to assess the expected performance distribution under uncertainty stemming from sparse inputs.



Benefits from executing LLM's with Anda over FP execution



SNN-STDP for attention-based people detection

Efficient Large Language Model acceleration

Large language models (LLMs) are becoming widespread, yet are extremely compute-intensive. Weight quantization has been pursued to reduce storage requirements, but this shifts the energy and latency bottlenecks to the memory access and computations of the costly floating-point (FP) activations and the KV cache. To tackle this, MICAS has been working on several HW-SW co-optimized innovations. On the one hand, a new data type has been proposed for activations, accepted for publication at HPCA2025: The Anda data type has an adaptive mantissa length with a group-shared exponent. Together with Anda-enhanced processing unit, it brings a 3.1× energy-efficiency improvement and a 2.4× speedup for popular LLMs like OPT and LLaMA. We further complement this with enhanced KV cache compression scheme to speed up both the encoding and decoding stage of modern LLMs.

Spiking and neuromorphic edge processing with continual learning

Traditional approaches for processing sensing data are energy-hungry. Inspired by biology, the MICAS team has been exploring alternative solutions that exploit the spiking and event-based nature of the signals. Spiking signal preprocessing in combination with spiking neural networks (SNNs) are significantly more energy-efficient in their implementation, making them affordable for local in-sensor processing and a better solution for many IoT applications and edge devices. An important aspect is the continual learning capability, where the system - with limited or no pre-training - continuously learns and improves itself from the inputs received through STDP learning. Demonstrated for the application of attention-based people detection by self-learning SNNs in autonomous drones, this work has been published at the 2024 NICE conference, in the IEEE Transactions on Cognitive and Developmental Systems and in detail in a book with Springer.

Contact

Hardware-efficient AI and ML

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"Customized multi-accelerator architectures are driving the rapid evolutions in artificial intelligence. MICAS is proud to perform at the forefront of this trend and keeps pushing the boundaries of the SotA."

Interested to read more?

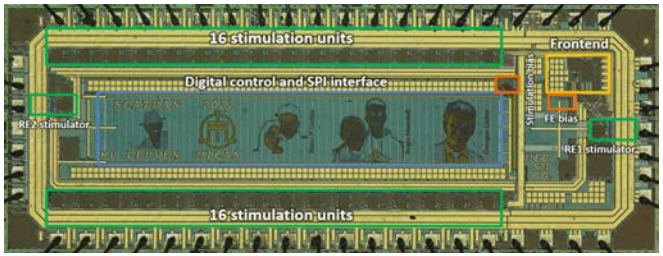
Check out our website for a detailed overview of all research topics in this domain.

Biomedical circuits and sensing interfaces

"The research at MICAS explores innovative chip implementations and hardware solutions for biomedical applications and sensing readout."

MICAS performs research on innovative integrated circuits and hardware solutions with application in all possible fields. Two crucial application domains that receive special attention are sensing readout and biomedical. Indeed, sensors are the front door bridging the physical world with the electronics world. Multimedia, augmented/virtual reality and the metaverse, modern cars, in-house heating and entrance control, robotics, current manufacturing plants, etc. are some of the many examples where sensing and imaging are employed ubiquitously. Enabled by the increasing capabilities of (wireless) communications, like the Internet of Things, distributed sensing devices have recently become key to constructing smart system applications, like smart cars, smart mobility, smart houses, smart offices, smart cities, smart manufacturing, smart farming, environmental monitoring, etc. Challenges in the design of the sensing readout involve the relentless reduction of the power and silicon area, while achieving increased performances in terms of sensitivity or dynamic range. The large amount of data generated in the sensing also calls for increased local data processing or computation "in the edge" to limit the communication cost. The second application field that has always been of special interest in MICAS is biomedical. Electronics offer huge opportunities towards improved diagnosis, increased monitoring, therapeutic stimulation, targeted drug delivery and more personalized medicine in general, saving and/or improving lives. Biomedical devices today range from large to handheld equipment and from wearables to implantables and ingestibles. Electronics not only allow for miniaturization but also add intelligence and customization capabilities. For several decades and years to come, the research at MICAS has been exploring improved chip implementations and innovative hardware solutions for biomedical applications, often in collaboration with medical doctors from the university hospital.

2024 highlights on biomedical circuits and sensing interfaces

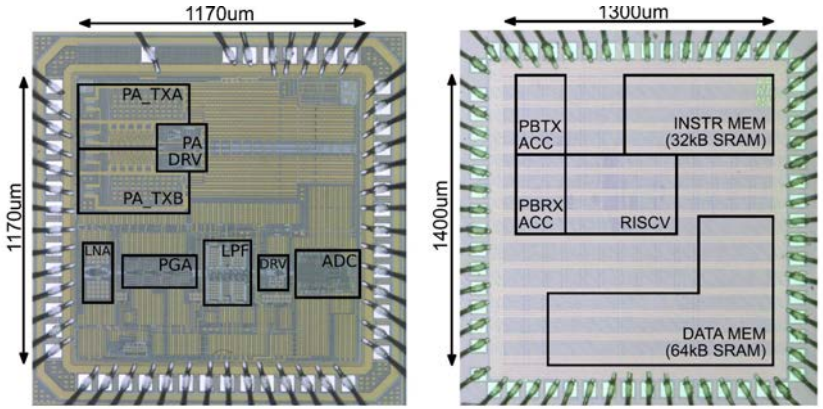


SCATMAN: a fully integrated chip solution for neural monitoring and stimulation in stroke-induced cavities

Closed-loop neuromodulation (with both monitoring and stimulation) is emerging as a more effective solution for the treatment of neurological symptoms, such as the treatment of abnormal neural behavior near stroke-induced brain cavities. A challenge is the ability to continuously record brain activity during electrical stimulation, due to the large artifacts that can saturate the sensitive readout circuits. A proof-of-concept chip in 180 nm CMOS has been developed containing multi-channel stimulation and a multi-channel multiplexed readout frontend with rapid artifact recovery that needs to be combined with backend linear interpolation to reconstruct the artifact-corrupted signal features. The chip contains time-domain conversion using a novel 13-bit incremental ADC and requires a record minimum area of only 0.0018 mm2 per channel, while consuming only 4.51 µW per channel. The work is an ideal candidate for integration in high-channel-count true closed-loop neuromodulation systems and has been published in the IEEE Transactions on Biomedical Circuits And Systems in 2024.

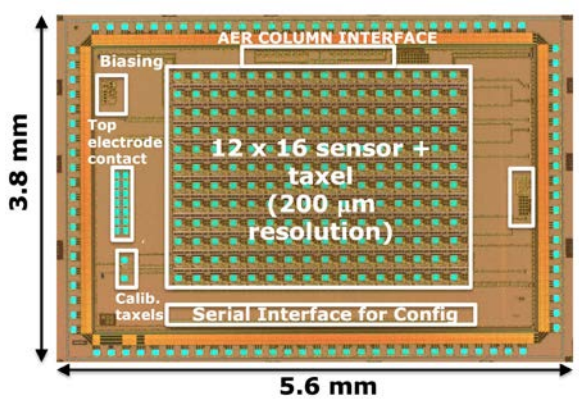
Circuit innovations for biomedical sensing readout

MICAS continuously explores and proves the feasibility of novel circuit innovations for biomedical sensing readout applications.In 2024, the capabilities and limitations of nanopore readout have been explored further. A high-speed readout for nanopore-FET (NPFET) sensor arrays has been developed, intended for high-throughput DNA or protein sequencing. The readout interface utilizes a novel architecture that can simultaneously perform recording and automatic background calibration to compensate for offset and drift of the individual NPFET threshold voltages. An 8-channel chip has been prototyped in 0.18 µm CMOS and published in the IEEE Transactions on Circuits and Systems I. A theoretical analysis of the detectability limits of single proteins in nanopore-based voltage and ionic-current sensing. It uses macromodeling to explore the detection limits. The work has been published in the ESSERC 2024 conference and an upcoming paper in the IEEE Sensors journal.



Ultra-sound modem for in-body communication.

In 2023 we had published a dual-chip ultra-sound modem for communication between implants in the human body. It can also communicate between skin and implant. The maximum bitrate is 470 kbps with a BER of $3e^{-4}$ without any form of error correction. In 2024, we have designed this into a single-chip modem in a 55 nm HV technology. The new modem will be taped out in the beginning of 2025 and will be extended with a wake-up receiver and extra digital processing blocks to further optimize the energy efficiency. Once validated, this will be a breakthrough for high-speed communication between and to biomedical implants. The next step will be to provide the modem with ultra-sound power.



A fingertip-mimicking high-resolution e-skin readout chip

Electronic skin (e-skin) solutions are important for the design of prosthetic or robotic hands with human-like tactile capabilities. MICAS has designed a taxel readout chip in 0.18 µm CMOS technology that achieves a record-high spatial resolution of 200 µm, comparable to human fingertips. A key innovation is the on-chip integration of a 12x16 taxel array with a per-taxel signal conditioning frontend and spiking readout combined with embedded neuromorphic first-order processing through Complex Receptive Fields. Experimental results show that classification of the chip's spatiotemporal spiking output with a low-bit spiking neural network achieves excellent accuracies up to 99% for input tactile stimuli such as texture. The chip achieves a state-of-the-art power consumption per taxel of 12.33 nW. It has been described in the IEEE Transactions on Biomedical Circuits And Systems. Currently, a design with larger taxel area in active TFT technology is being validated.

Contact

Biomedical circuits and sensing interfaces

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"Challenges in the design of the sensing readout involve the relentless reduction of the power and silicon area, while achieving increased performances in terms of the sensitivity or dynamic range."

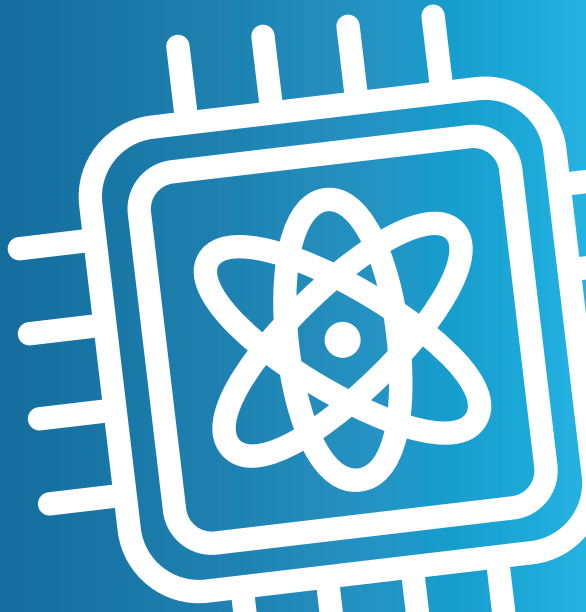
Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

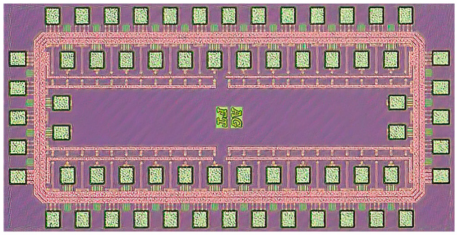
Quantum and cryogenic circuits

"Solid-state circuits to control and observe a growing number of quantum devices will be essential."

Quantum technologies, including computing, sensing, communications, information technology, and security, are rapidly emerging thanks to the combination of future challenges in these domains and recent advancements that enable quantum technologies to provide an answer. Densely integrated solid-state circuits to control and observe the growing number of qubits will be essential in successfully realizing such technologies. Since most quantum technologies rely on deep cryogenic temperatures, chips must also operate at those ultra low temperatures to ensure compact, reliable, and, especially, scalable systems. The Einstein Telescope, the next-generation gravitational wave detector currently under development, also requires cryogenic operation and, thus, cryogenic circuits. MICAS is involved in all these initiatives, and it also has invested in the necessary cryogenic measurement infrastructure.



2024 highlights on quantum and cryogenic circuits



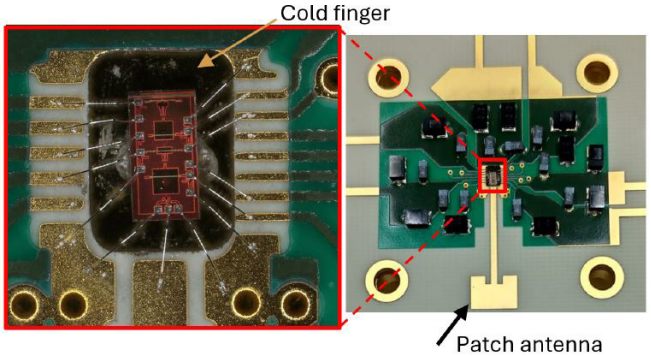
Cryogenic Scalable Compact Transistor Model

The behavior of transistors at cryogenic temperatures differs significantly compared to room temperature. Moreover, this cryogenic behavior is not modeled in regular PDKs. We have extensively characterized the transistor performance at these extreme temperatures with the aim to construct our own cryogenic transistor model. This has resulted in our first paper in the IEEE Journal of the Electron Devices Society in which we present the cryogenic characterization and compact modeling of thin-oxide MOSFETs in a standard 65 nm Si-bulk CMOS technology. The influence of both short- and narrow-channel effects at extremely low temperature on key device parameters such as threshold voltage and ON current is highlighted, and the performance of this technology node for cryogenic analog circuit design is discussed. It is then demonstrated that the BSIM4 parameter editing approach can be successfully used to model small dimension effects at cryogenic temperature. In the absence of cryogenic foundry models, the robustness and simplicity of this modeling technique make it a preferred method to quickly build a design-oriented, fully scalable SPICE compact model. This restores complete freedom in device sizing for cryogenic analog circuit design and enables us to develop complex analog and mixed-signal chips with good reliability.

Our first cryo-ADC for qubit readout

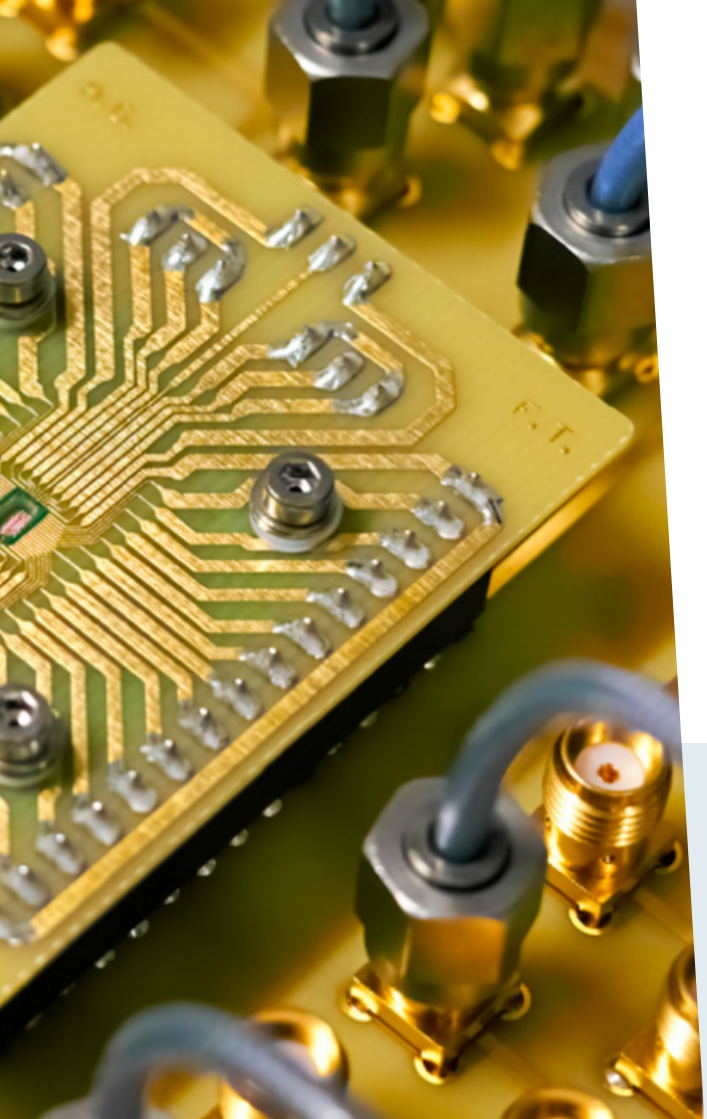
Cryogenic temperatures offer several opportunities for analog and mixed-signal chips. For example, the carrier mobility and the subthreshold slope increase, while thermal noise decreases. This enables a completely new approach to implementing circuits compared to the one that is typically used at room temperature. For example, an ADC is typically designed to cope with thermal noise resulting in a certain minimal power consumption. However, this limit is almost non-existent at 4 K, the cooling stage temperature of a cryostat with reasonable cooling capacity.

We have developed a cryo-ADC with only 4 fF input capacitance, which would be impossible at room temperature due to the thermal noise limit. Such an ADC is extremely easy to drive, which brings several benefits for the quantum computing system that will use it. The ADC has been implemented in a 40 nm CMOS technology and is presented at ISSCC 2025.



Mm-wave cryogenic oscillators

This research investigates the design, implementation and measurement of mm-wave oscillators for cryogenic applications. Reading out qubits at higher temperatures might require higher clock frequencies, going up to mm-wave frequencies, while achieving extremely low jitter, phase noise combined with low power dissipation. In 2024, several mm-wave oscillators have been designed in 40 nm CMOS and measured down to 4 K using a wireless measurement technique with a patch antenna on PCB. These experiments are used to validate the models, design techniques and measurement approach and will be continued to develop complete readout frontends that operate at cryogenic temperatures.



Contact

Quantum and cryogenic circuits

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"Quantum and cryogenic circuit design provides exciting new challenges for proven and scalable CMOS technologies."

Interested to read more?

Check out our website for a detailed overview of all research topics in this domain.

Educating for excellence

We train and guide talented **PhD** and **postdoctoral students**, to become trendsetters in micro- and nanoelectronics.

We involve **bachelor** and **master students** who are passionate about the world of chip design in our projects.

Training experts at the bachelor, master, PhD and continued-learning levels

Bachelor

MICAS supports bachelor education in Electrical Engineering at KU Leuven. In this curriculum, students are trained in the broad range of electrical engineering subjects, and are learning the fundamentals in the field, with a strong mathematical foundation. The MICAS professors offer education in electronic circuit design and digital implementation. Every year, about 100 new bachelor students join this program.

Master

Within the master in Electrical Engineering at KU Leuven, one of the tracks specializes on chip design, training tomorrow's IC designers. Master students enrolled in the program are trained by the various MICAS professors on all different aspects of chip design, ranging from analog and mixed-signal design, over RF and mm-wave circuits, to digital implementations and processor architectures as well as CAD. Every master student also performs a deeper study on one subject in her/his master thesis, and as such already gets a taste of the MICAS research culture.

PhD

MICAS houses more than 70 PhD students, maturing to become true experts in their fields. An important aspect of their work is to explore innovatively new circuit solutions, but also to validate these concepts experimentally through actual chip implementations. In addition, the PhD students are not only trained to excel technically, but they also get educated in effective communication, creativity, teamwork, paper writing, and student supervision. As such, we are proud to train the change makers of the future in the world of chips.

Continued-learning micro-credentials

In 2024, MICAS has organized a series of micro-credential courses together with several leading companies in the field. These micro-credentials enable both students and professionals to up-skill and re-skill themselves in the field of analog and digital chip-development. The courses cover a range of industry-relevant competences that allows both experts and novices to start or continue a career in chip design and development. The micro-credentials will receive an extra boost, both in terms of content and in expanding their reach, thanks to the creation of the Flanders Chips Competence Center, an initiative supported by the European Chips Joint Undertaking and the Flemish government, and coordinated by MICAS.

What appeals students at MICAS?

Why do PhD and master students like studying and working at MICAS? What makes MICAS/ KU Leuven a good place for them? What opportunities does it bring?

We asked them these questions, which resulted in a variety of answers ...

"You can work with many international researchers having various backgrounds in the field of electronics. A lot of opportunities to design a chip in advanced technologies, to collaborate with world-wide companies and with imec."

Kodai

"MICAS gives you the opportunity to go through the entire chip design cycle from idea, design, manufacture to actually measure your own integrated circuit(s)."

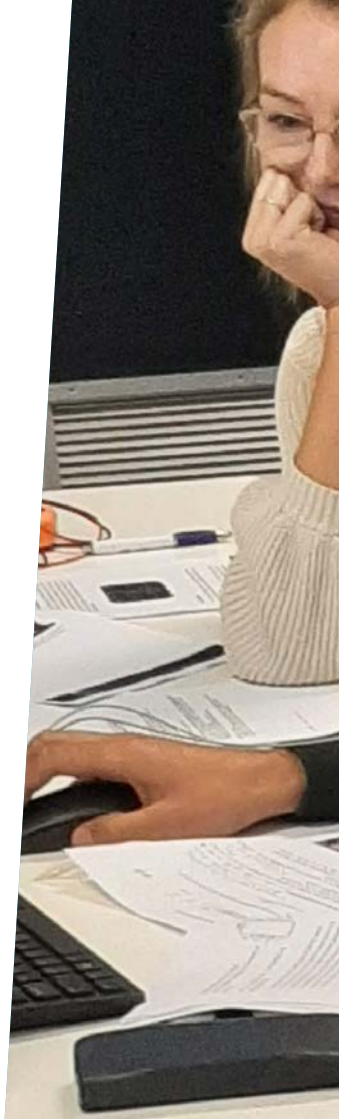
Thomas

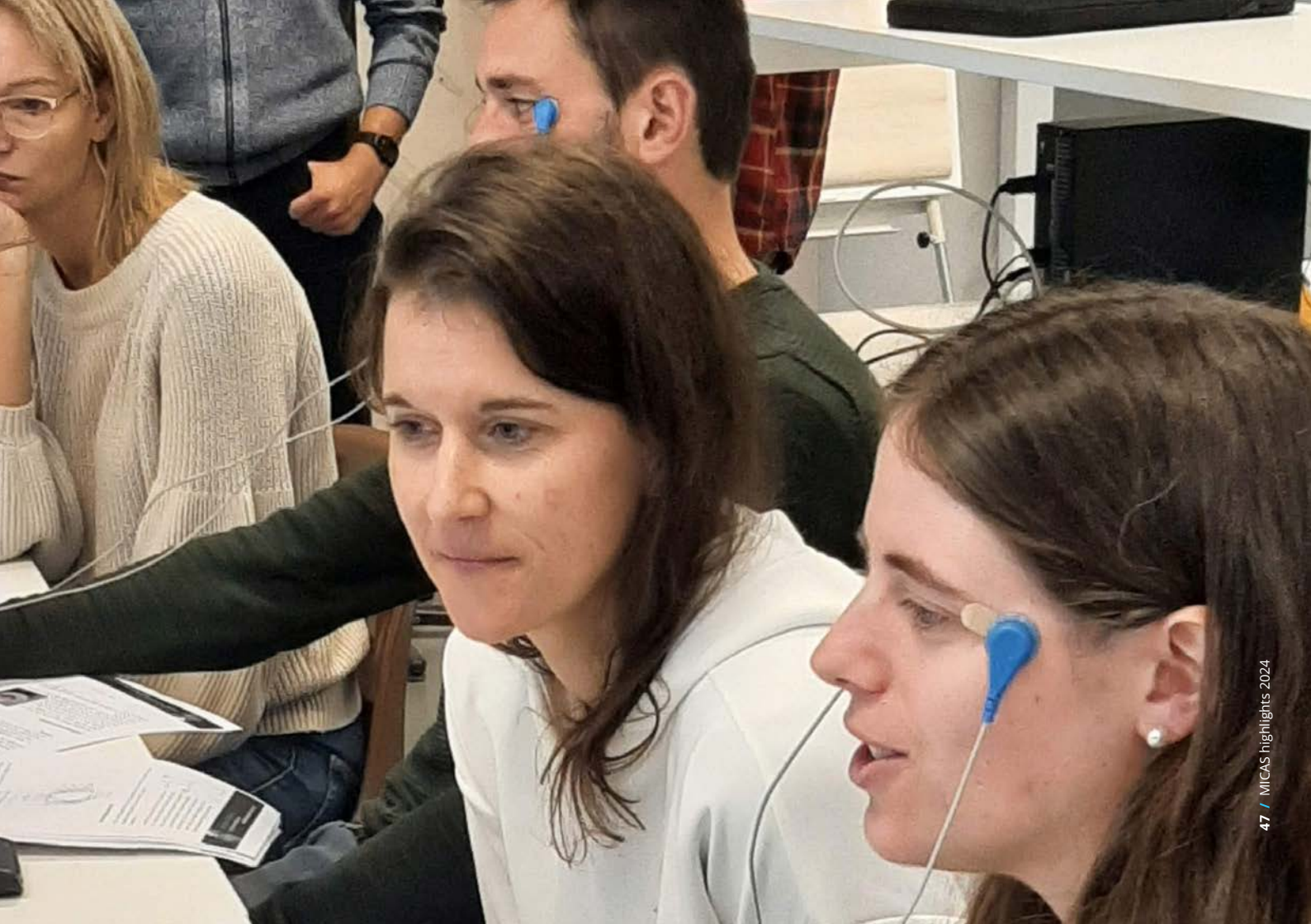
"At MICAS, I experienced unprecedented creative freedom, allowing me to substantially broaden my knowledge, enhance my skillset, and engage in the most advanced research within my capabilities, all within a supportive and enjoyable community of like-minded individuals."

Carl

"A unique mixture of creativity, freedom, and knowledge topped with some funny craziness."

Tim





Inspiring society

Besides education and research, MICAS also sees it as its core task to inspire others.

This includes inspiring youngsters towards a career in STEM or micro-electronics; inspiring society towards the opportunities that come from ubiquitous electronics; and being a continued source of inspiration for our alumni to keep developing electronics in applications that matter. We are proud to discuss some recent initiatives in these areas.

> "Making society aware of the importance of microelectronics and resulting opportunities."

> "Enthusing others to actively participate in the shared mission of using STEM and micro-electronics towards a better society."

OUTREACH

We not only publish our research output in peer reviewed scientific journals, but we also write articles for magazines with a broader audience. In this way, we inform the more general public about our realizations and about the opportunities of our research.

We also use other channels to reach out to a broad audience, from television to social media, live science debates and podcasts. Prof. Marian Verhelst is a regular guest in the monthly science podcast "Nerdland", which discusses (in Dutch) the scientific breakthroughs of the month to non-experts. This podcast consistently ranks within Spotify's list of most popular podcast in Flanders.

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STEM

STEM disciplines (**S**cience, **T**echnology, **E**ngineering and **M**athematics) struggle to attract sufficient students to cover the need of the job market. One of the root causes of this problem seems to be the difficulty to link the abstract study fields of science and mathematics with the practical application and relevance of these disciplines in our day-to-day lives.

To overcome this, MICAS leads multi-partner projects like the educational network 'iSTEM' and InnovationLab. With these projects, we aim to not only enhance the STEM literacy of youngsters, but also to improve their attitude towards STEM and its role in society.

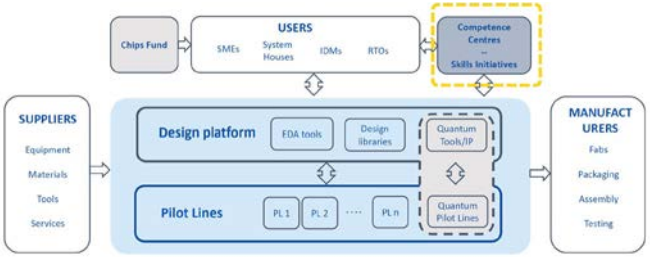
InnovationLab: The link between technology and the impact on people's daily life takes a central role in the vision of InnovationLab, which offers fully developed STEM projects in which students tackle a societal challenge (https://eng.kuleuven.be/innovationlab/). Each InnovationLab project can be carried out at the secondary school itself, by the school's own teachers, using the material provided by InnovationLab. On these project days, students can experiment, investigate, and practically engage themselves in real engineering tasks.

iSTEM: The activities of iSTEM range from secondary-school teacher professionalization and inspiration to coaching. On the website (www.istem.be) teachers find, among other tools and inspiration, more than 50 projects which they can adapt to their everyday class practice (creative commons license). On top of the intensive courses and workshop teachers can attend weekly iSTEM nocturnes, where each time one of the projects is highlighted. On top of the tailor-made coaching activities of teacher design teams, schools can now enroll in a comprehensive trajectory to strengthen their STEM education.

Formation of the FLANDERS CHIPS COMPETENCE CENTER

In the course of 2024, professor Patrick Reynaert, in close collaboration with our research valorization manager David Maes, has taken the lead in defining and implementing a new organization that will form a cornerstone in the Chips for Europe Initiative. The so-called Flanders Chips Competence Center (FC3) will act as a service and skill development organization, complementing the Design Platform, the Pilot Lines, and the Chips Fund, which are also in development in the same Chips for Europe framework. The FC3 will be the first point of contact in Flanders to facilitate access to these instruments and infrastructure, and to technical expertise in the fields of chip development and system integration. It also aims to be instrumental in alleviating the talent shortage in the broad semiconductor ecosystem. To reach its goals, the FC3 will deploy five major activities:

1. providing skill development, mainly by organizing courses
2. offering chip development and system integration services, both for mature technologies, as well as for upcoming technologies
3. creating pathfinding demonstrators, as a means to showcase the potential of chip technology
4. acting as a central contact point, functioning as a proactive front office towards all the stakeholders and potential clients of the center
5. outreach and dissemination, to have a bidirectional interaction between the center and the public



The focus area of the FC3 is the broad domain of analog, mixed-signal and digital chip design and development, photonic components, chips and technology, and electronic and photonic system integration. The FC3 consortium partners are KU Leuven, Ghent University, Vrije Universiteit Brussel, and University of Antwerp. Their expertise in skill development, chip design, and system integration, combined with its strong ties to industry, its world-class infrastructure, its innovative R&D models, its active support for entrepreneurship, and its well-developed relationships with the other stakeholders of the Flemish and the European chips ecosystems, will form a solid basis on which this new initiative can become successful. Similar centers are being set up in other EU member states, forming a European Network of Chip Competence Centers.

The FC3 will be funded by the European Commission and by the Flemish Government. It will kick off its activities in the beginning of 2025. More information can be expected very soon.

Spin-offs

Disruptive research opens up new markets, not yet covered or under development in existing companies. This is where entrepreneurship within MICAS meets research. MICAS is very successful in this model, leading to the creation of on average one spin-off company every four years.

The total amount of employment to date due to these spinoffs is over 300 full-time employees, mostly highly skilled IC designers and electronic-system engineers. Since most of these companies are located near KU Leuven, this creates a local Silicon Valley ecosystem in the Leuven area. These spin-offs regularly operate in close collaboration with KU Leuven and the MICAS researchers.

TUSK IC

2018

research and product design solutions in the field of mm-wave IC design

www.tusk-ic.com

MDA
Mephisto Design Automation

2006

analog, mixed-signal and custom digital design automation solutions

Liquidated in 2011

2016

advanced measurement solutions for various industries, providing precise, reliable, and efficient measurement systems

www.hammer-ims.com

2015

design of radiation-hardened integrated circuits

www.magics.tech

2011

mixed-signal IC design company, developing power management ICs

www.mindcet.com

2007

design house for electronic engineering, offering a complete range of consultancy and engineering services

Acquired by Comate in 2022

2004

analog, high-voltage, mixed-signal ASIC design and supply

www.icsense.com
Part of the TDK group since 2017

2003

analog design software, including modeling, sizing and layout tools, addressing high-complexity analog functional blocks

Acquired by Magwel in 2008

1998

custom mixed-signal IC design and turnkey ASIC solutions

www.ansem.com
Acquired by Cyient in 2018

1981

computer-aided design software for simulation and lay-out of ASICs

IPO in 1984 – Acquired by Mentor Graphics in 1990 – Spin-out as Frontier Design in 1997 – Part of Adelante Technologies in 2001 – Acquired by ARM in 2003

Events

MICAS Alumni and Friends Events

In 2024 we had again two different 'MICAS Alumni and Friends' Events. The first one took place at the occasion and at the location of ISSCC in San Francisco, with Flanders Investment and Trade (FIT) as host and sponsor of the event, for which we are very thankful!

The second one was in November, not so far away: in De Oude Kantien. It is always nice to see that so many of our alumni and other friends take to time to meet, interact, discuss, and have a drink together. The MICAS community shows to be a vibrant network of people active in industry or academia. Next edition of 'MICAS Alumni and Friends' at ISSCC 2025!

A look back at ESSERC 2024

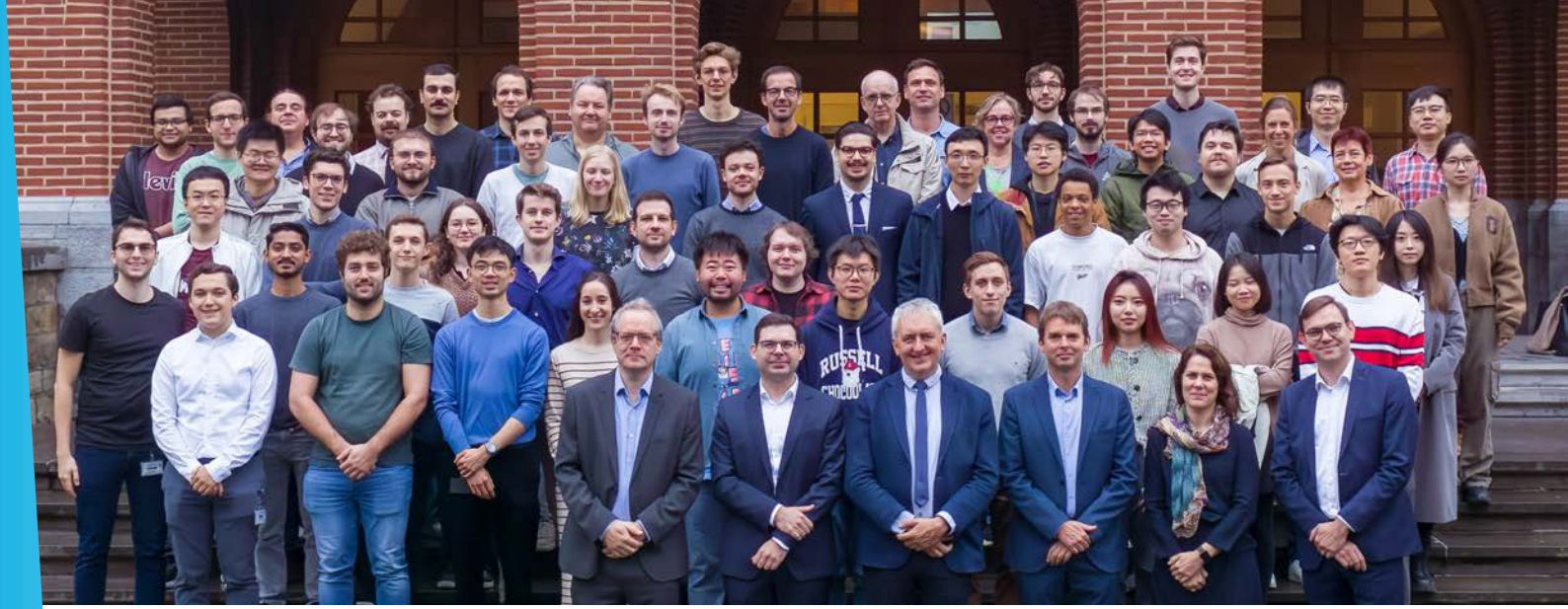
2024 was also the year in which we organized the European Solid-State Electronics Research Conference (ESSERC), in the beautiful city of Bruges. It was the 50th edition of the conference. ESSERC was established by merging the European Solid-State Circuits Conference (ESSCIRC) and the European Solid-State Device Research Conference (ESSDERC), reflecting the growing intertwining of circuit design and device technology, aiming to stimulate the collaboration among technologists, device experts, IC designers, and system designers.

ESSERC 2024 brought us excellent scientific contributions, highly interesting plenary sessions, with lots of interaction from the audience. There were plenty of networking opportunities, with the reception at the Brouwerij De Halve Maan and the diner at Lauretum as clear highlights. The vibrant atmosphere and the many informal contacts made it very clear that physical meetings remain irreplaceable.

Hope to see you all in Munich for the 51st edition of ESSERC!

MICAS team

MICAS is a close-knit, collaborative team of professors, researchers, and support staff, striving for excellence, “pushing ourselves to deliver the highest-quality performance in everything we do”



- **6 professors**, each excelling in his or her discipline, skills and expertise acquired at academic institutions, industrial multinationals, or a combination of both, domestically and abroad;
- **70 PhD** students and **postdocs**;
- **12 technical and support employees** to coach and help researchers on the use of design and measurement infrastructure, and to assist the whole team in matters related to HR, finance, IT, and tech transfer.

Academic staff

Wim Dehaene

Main research topics:

- Circuit-level digital design
- Low-power digital circuits
- Biomedical circuits
- Design in TFT technology

Georges Gielen

Main research topics:

- (Beyond-)CMOS analog and mixed-signal ICs
- Data converters and sensing interface circuits
- Analog/mixed-signal CAD tools and design automation
- Testing of analog/mixed-signal ICs

Patrick Reynaert

Main research topics:

- Power amplifiers
- Mm-wave and THz CMOS circuit design
- High-speed and broadband circuits

Tim Piessens

Main research topics:

- Sensor interfaces
- High-voltage circuit design
- Mixed-signal circuits and data converters

Filip Tavernier

Main research topics:

- Circuits for optical communication
- High-speed wireline communication
- High-speed A/D&D/A converters
- Fully integrated power management
- Radiation-hard IC design

Marian Verhelst

Main research topics:

- Chips for machine learning and AI
- Computer architectures
- Low-power, embedded processing
- Context-aware, ubiquitous electronics

MICAS Emeriti

Michiel Steyaert

Main research topics:

- Power management and DC/DC circuits
- RF CMOS and telecommunication circuits
- Wireline and optical communication circuits
- Analog signal processing and A/D and D/A converters

Bob Puers

Main research topics:

- Medical implants for monitoring and stimulation
- Sensors and actuators
- Silicon and polymer MEMS
- Biocompatible packaging and interconnection
- Biotelemetry and inductive powering

In Memoriam Willy Sansen

This past year, we have had to cope with a profound loss: our founder and shining example, Willy Sansen, passed away on April 25, 2024.

In one sentence, Willy Sansen's research can be summarized as: enabling systematic analog circuit design in a digital, CMOS dominated, world. He has shown how to start a design from transistor-level models, founded in solid-state physics, move on to building blocks like opamps or OTAs, and finally end up in fully integrated analog systems, such as filters, A/D-D/A converters, and all other kinds of analog signal processing blocks. Willy Sansen was one of the founders of this systematic approach. In the eighties, a time where almost all design went digital, Willy Sansen kept investing in analog research. His vision was that, the more accurate and high-performant the digital processors become, the more accurate and high-bandwidth analog signals will be needed. A vision that materialized in the last decades.

Analog building blocks and their systematic design are definitely the central theme in Sansen's research, but he also cared for the relevance and application of analog circuits. That is where his love of biomedical electronic systems came from. Willy was the driving force behind the design of an early platform for a biomedical measurement and stimulation system: the Internal Human Condition System (IHCS). He was broadminded enough to incorporate the digital innovations of those days on it: a microprocessor! Willy Sansen was also a pioneer in the development of fully integrated stimulation drivers for the early cochlear implants.

Willy Sansen was at the same time a gifted teacher. Anyone who ever attended one of his classroom lectures, or one of his conference speeches, will forever remember it. His charismatic style was fascinating and inspiring. For the content of his classes, as for his research, systematic is also the keyword. Willy Sansen understood the art of building concepts that students initially experience as difficult – circuit stability is a good example – from the ground up, highlighting the basic principles and gradually increasing the complexity. At the end of the road, as the student or attendee, you just saw the light! His talent and drive for education has culminated in the book "Analog Design Essentials" (Springer, 2006). Most probably the bible for many generations of analog circuit designers to come. Willy was also innovative when it came to educational technology. Decades before the pandemic forced everyone to record classes, Willy Sansen already made his courses available on video tape. Sansen was teaching at KU Leuven, Belgium, from 1972 till he became an emeritus professor in 2008. But Willy Sansen was not only teaching on the home front: he must have flown many times around the globe to visit universities and companies almost everywhere on earth to educate and to inspire students and starting engineers in analog circuit design.

Willy Sansen has always been playing at international level. His Berkeley PhD laid the foundations for an international network that spans the globe. Throughout the years, he was a visiting professor in Philadelphia, Pennsylvania (USA), Ulm, Villach and Munich (all Germany). He has been on the technical committees of many conferences. He became even the first European program chair (in 2002) of the International Solid-State Circuits Conference (ISSCC), the most prestigious conference in IC design. Later on, in 2008-2009, he served as the first European president of the IEEE Solid-State Circuits Society (SSCS). Willy Sansen received many awards and honors in his career, from academy and industry, but the most distinctive award, and the one he was most proud of himself, is the 2011 IEEE SSCS Donald O. Pederson Solid-State Circuits Award.

When Sansen retired from active duty at KU Leuven in 2008, having supervised 65 Ph.D. theses and having (co)authored more than 650 papers and 16 books, he left behind a well-established research group: MICAS. It is our challenge to maintain and further develop the high standards set by Willy Sansen and to let him live on in our ever-continuing research towards integrated "circuits for a better life".

by W. Dehaene, M. Steyaert, G. Gielen,
P. Reynaert, F. Tavernier, M. Verhelst

Retirement of Michiel Steyaert

On October 18th we celebrated the retirement of MICAS staff member professor Michiel Steyaert. In a very entertaining academic session, KU Leuven rector Luc Sels, KU Leuven Faculty of Engineering Science dean Jos Vander Sloten, former Department of Electrical Engineering chair, former vice-rector and MICAS staff member Georges Gielen, Delft University of Technology professor Klaas Bult, and MICAS staff member Patrick Reynaert each highlighted from their own personal perspective the impact that Michiel has realized throughout his academic career, in his role as dean, as department chair, but also outside the university.

At the event, it was announced that Michiel has been awarded the IEEE Donald O. Pederson Solid-State Circuits Award, a firm recognition for his pioneering contributions to RF CMOS circuits and integrated power converters. In his closing speech, Michiel especially brought a message of thankfulness for all the enjoyable interactions, fruitful collaborations, and the many opportunities that have crossed his path. Michiel, this feeling is mutual. Thank you for your enormous influence on the MICAS research and its societal impact! We will reap the benefits of this for a long time to come.

Introducing prof. Tim Piessens, the engineering educator

On October 1, 2024, Tim Piessens started as a professor at MICAS. Prof. Tim Piessens embodies the fusion of fundamental insights, technical innovation, and practical application. Transitioning from CTO at ICsense, a successful MICAS spin-off, to a professorship at KU Leuven, Tim bridges the gap between industry and academia. This move reflects his passion for engineering, research, and education. Tim sees his new role as a "once-in-a-lifetime opportunity" to deepen his focus on technical subjects while training and mentoring the next generation of engineers. He brings with him a wealth of experience in efficient and meticulous design and mixed-signal modeling, paired with a commitment to promoting entrepreneurship among his students. By sharing real-world examples and lessons from his career at ICsense, he hopes to inspire curiosity – a quality he considers essential for any successful engineer. His research interests include ultra-low-power and high-precision sensor readout systems, essential for the growing field of smart sensors. Tim explores innovative concepts like frequency-domain multiplexing in this field. He is also delving into chaos theory and non-linear systems. Additionally, he is passionate about advancing the electrification of mobility, tackling challenges such as the need for high-precision and low-power circuits in the harsh automotive environment. A proponent of collaborative innovation, Tim emphasizes the importance of maintaining strong ties between academia and industry. He notes that while universities excel at high-risk, "blue-sky" research, they must also remain connected to industrial advancements to stay relevant. Spin-offs and entrepreneurship are central to his vision of academia's role in technological progress.

Outside of work, Tim enjoys volleyball, running, family outings, and board games. He draws inspiration from science fiction and music, appreciating their ability to stimulate creativity and provoke thought on societal issues. Tim credits his early curiosity – disassembling objects as a child – and his family's encouragement for his lifelong passion for engineering. Looking ahead, Tim is both optimistic and cautious about technology's societal impact. While advancements in fields like health monitoring and automotive electrification offer tremendous potential, he stresses the need for critical reflection on ethical and social implications. Engineers, he believes, must balance innovation with responsibility, ensuring their work contributes to a sustainable future.

Read more about prof. Tim Piessens on our website.

PhD Graduates 2024

Steven Colleman

Modeling and Analysis for Efficient Hardware Mapping of Neural Network Algorithms

Promotor: Prof. Marian Verhelst

Ariane De Vroede

Terahertz Receivers in CMOS for Imaging Applications

Promotor: Prof. Patrick Reynaert

Gabriel Guimaraes

CMOS Terahertz Systems: From Circuits to Applications

Promotor: Prof. Patrick Reynaert

Bob Vanhoof

Ultra-low Leakage Power SRAM for Biomedical and IoT Applications

Promotor: Prof. Wim Dehaene

Joren Vaes

Polymer Microwave Fiber as a High Data Rate Channel

Promotor: Prof. Patrick Reynaert

Jonas Pelgrims

Circuit Design for Ultrasonic Haptic Feedback in Large Area Electronics

Promotor: Prof. Wim Dehaene

Jhon Gomez

Testing and Design for Testability of Latent Defects in Mixed-Signal Integrated Circuits

Promotor: Prof. Georges Gielen

Tuur Van Daele

Fully Integrated High-Voltage DC-DC and AC-DC Conversion

Promotor: Prof. Filip Tavernier

Ali Safa

Neuromorphic Sensor Fusion and Continual Learning for Drone Navigation and Radar Sensing

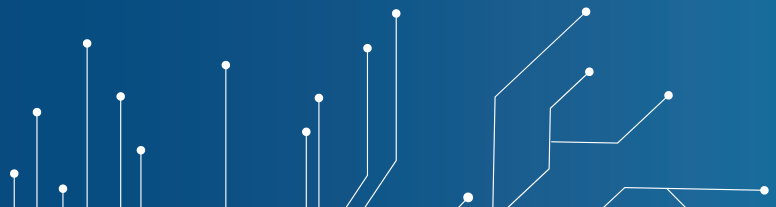
Promotor: Prof. Georges Gielen

Jonah Van Assche

Event-Driven Circuit Architectures for Scalable and Adaptive Sensor Readout

Promotor: Prof. Georges Gielen

Awards



MICAS Awards

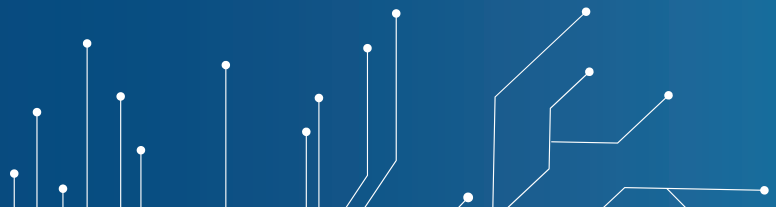
Michiel Steyaert received the **2025 IEEE Donald O. Pederson Award in Solid-State Circuits** "For pioneering contributions to RF CMOS circuits and integrated power converters." The highly regarded award reflects an individual's or team's exceptional achievements in advancing the frontiers of technology.

Marian Verhelst was selected as a member of the **Royal Flemish Academy of Belgium for Science and the Arts** (KVAB). The Academy develops science-based position papers, coordinates the Thinkers' Programme on grand societal challenges, and organizes colloquia, concerts and exhibitions.

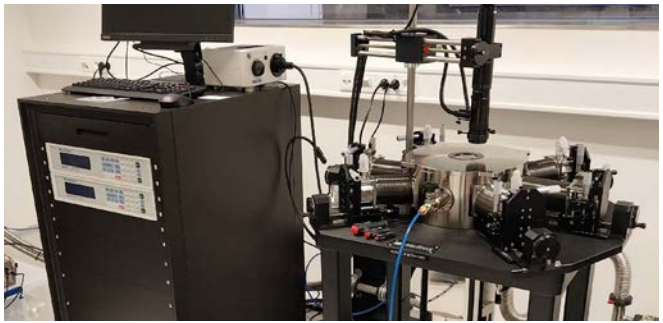
Alberto Gatti has received the Analog Devices, Inc. Outstanding Student Designer Award. The award, presented by ADI at the IEEE International Solid-State Circuits Conference (ISSCC), recognizes Alberto's outstanding research work on the design of cryo-CMOS circuits.

Labs, services & equipment

Our state-of-the-art in-house measurement and technology labs are crucial assets to experimentally validate our research results. The equipment is also available to companies or other research groups in a service model.



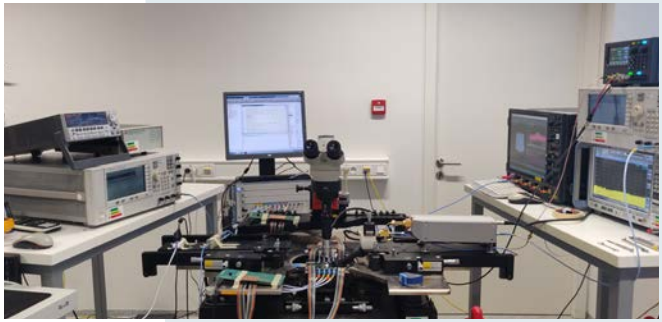
IC-Lab LF: low-frequency measurement lab



IC-Lab LF contains specialized equipment in the range from DC to several GHz. The main focus of this lab is on low-noise, high-resolution signal generation and power source analysis.

Recently we have invested in a cryogenic station and cryogenic probe station, enabling us to perform electrical characterization at cryogenic temperatures down to 3.2 K.

IC-Lab HF: broadband, optical, mm-wave and THz measurement lab



IC-Lab HF contains wideband measurement equipment such as signal analyzers, arbitrary waveform generators, oscilloscopes and vector network analyzers. An extensive set of high-performance instruments is available to ensure the best possible measurement accuracy up to frequencies well above 1 THz.

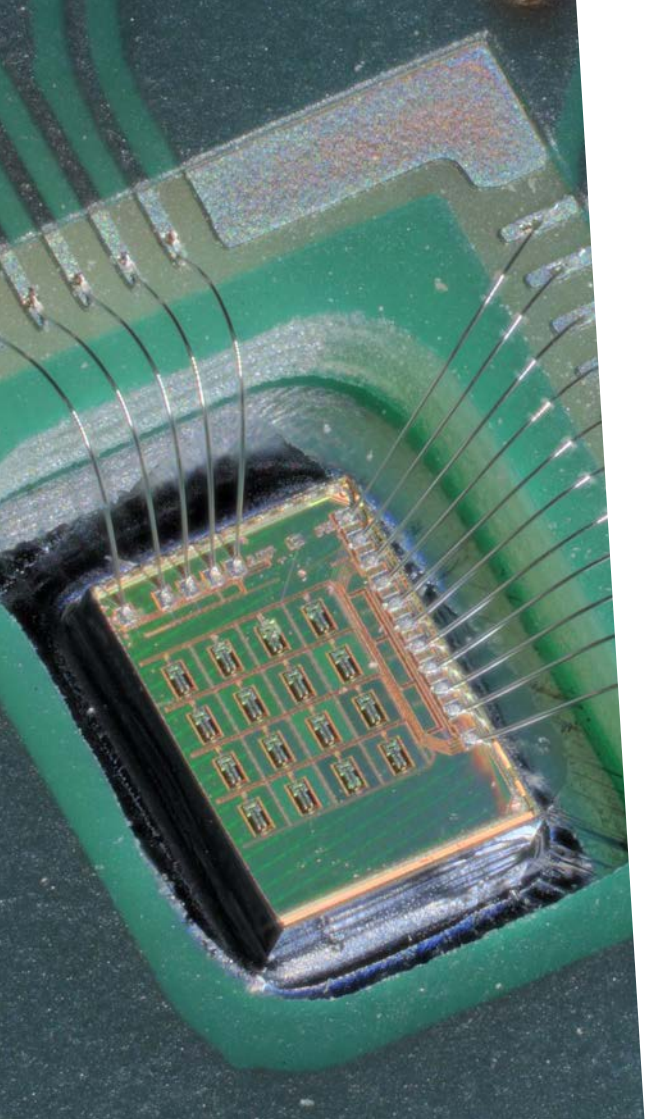
Thanks to the recently installed WR0.65 extenders, we can now generate and analyze signals up to 1.5 THz.

Technology Lab: chip packaging and modification facilities

In the MICAS Technology Lab, we have all the necessary chip packaging equipment such as dicing, bonding, and flip-chipping tools. For advanced chip modification, a specialized Focused Ion Beam system (FIB) is available.

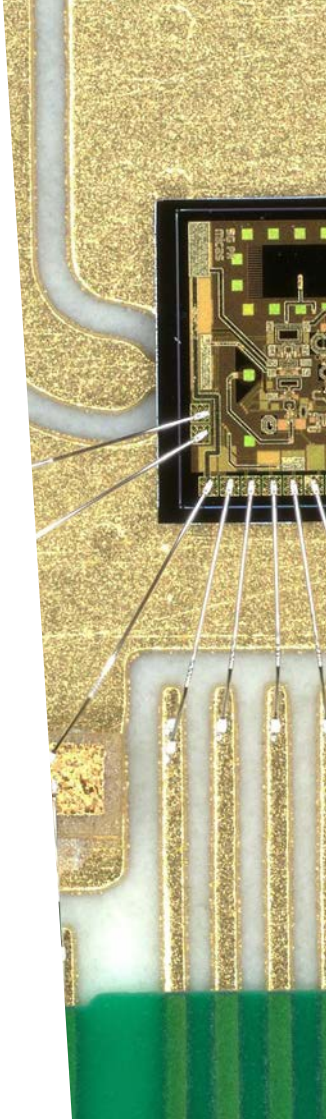
Dicing & grinding

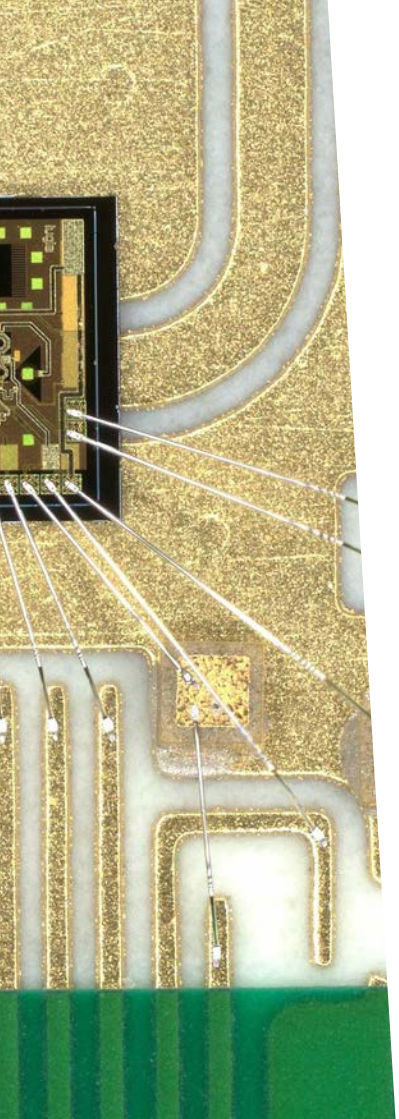
Our dicers can cut silicon wafers up to 300 mm in diameter and 0.8 mm in thickness. Glass wafers can be cut up to a thickness of 2 mm. We also cut dies that contain multiple designs into single chips. A specialized CNC-controlled grinding machine can perform decapsulation, silicon thinning and polishing of integrated circuits.

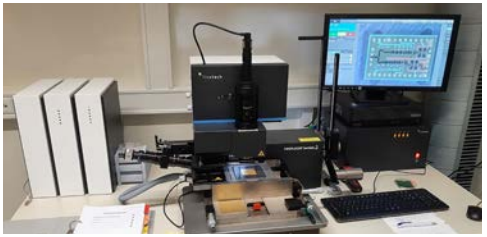


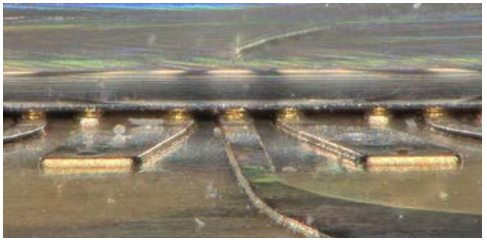
Bonding

The bonding lab is specialised in packaging small series of a wide variety of state-of-the-art chip designs. Wirebonding can be done with both gold and aluminium wires, either on a PCB or in a package.









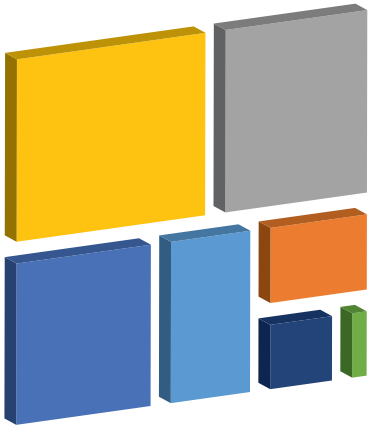
Flip chip

With our Finetech Lambda FINEPLACER machines, we can flip chips with gold studs as well as with copper pillars and solder caps. If needed, we can place the gold studs ourselves with our gold bonding equipment. For chips with up to 40 connections we can use a thermosonic flip chip process at moderate temperatures (~100°C), while for higher amounts of connections we use a thermocompression process at higher pressures and temperatures (up to 300°C).

Focused Ion Beam

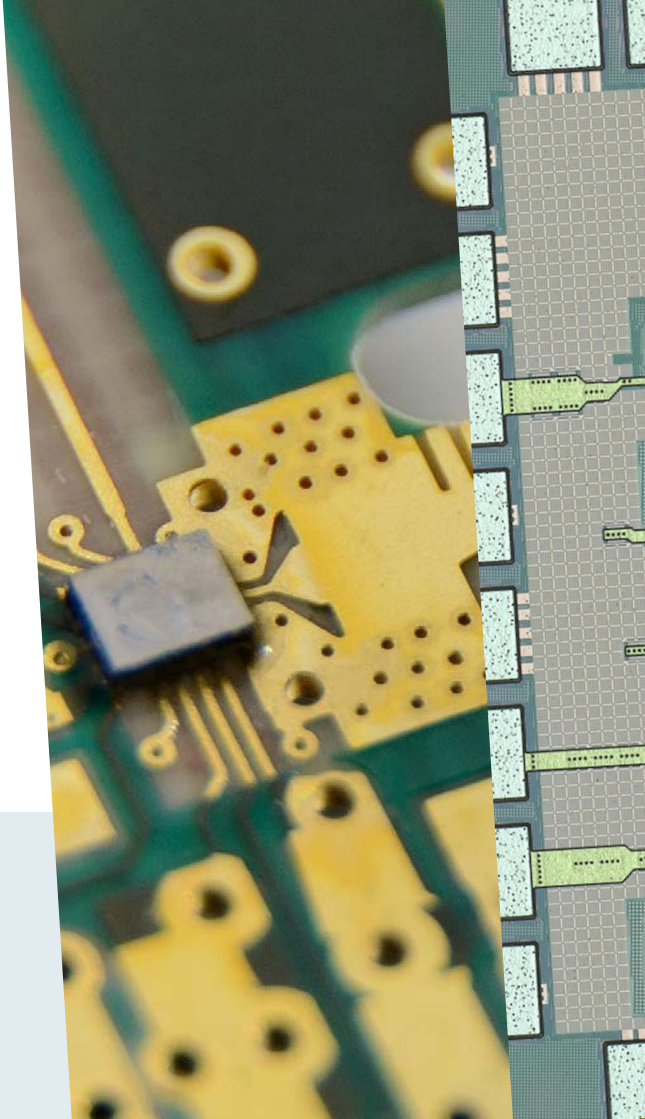
For advanced chip modification, a specialized Focused Ion Beam (FIB) system is available. Several materials can be removed and deposited with nanometer accuracy so that circuits can be modified without the need for re-processing. A unique feature of the system is the increased working distance so that electrical components around the chip do not hinder the repair operation. This allows us to not only make modifications on single dies, but even on dies mounted onto a PCB.

Chip gallery



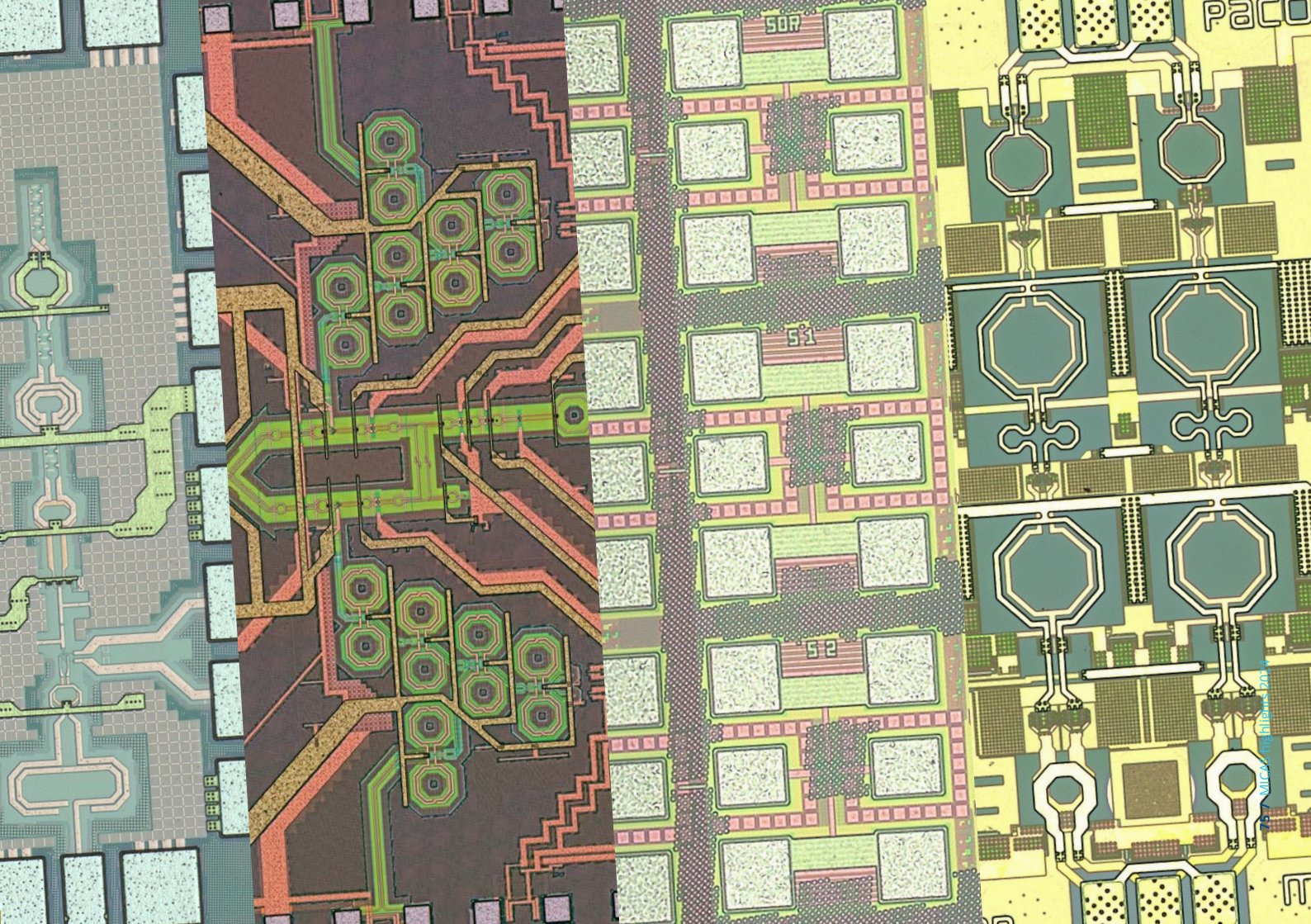
MICAS 2024 Tape-Out Area Per Technology

- TSMC 16nm CMOS
- Global Foundries 22nm FDX
- TSMC 40nm CMOS
- TSMC 65nm CMOS
- XFAB 0.18µm HVSOI
- Teledyne 250nm InP
- Pragmatic Helvellyn FlexIC



Interested to see more?

Check out our website for an overview of the chips that have been developed by our team since 2011.


SOA
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