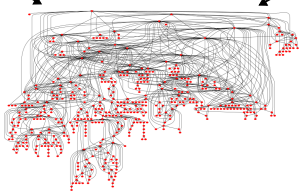
Probabilistic circuits (PC)

Sparse matrix triangular solves (SpTRSV)



Acyclic DFG

Optimization scope

Application

Compilation

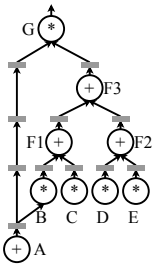
Hardware

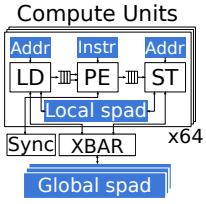
Implementation

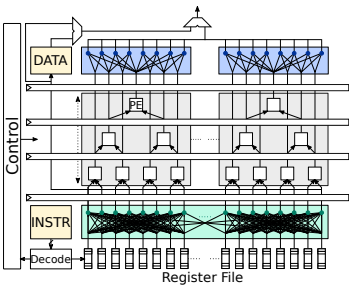
ProbLP & posit
chapter 2

GraphOpt
chapter 3

Targeted compiler
chapter 5







Fully-pipelined low-precision hardware

chapter 2

DAC 2019

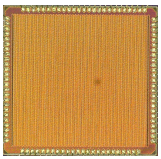
DAG Processing Unit version 1 (DPU)

chapter 4

DAG Processing Unit version 2 (DPU-v2)

chapter 5

MICRO 2022, DATE 2020



28nm CMOS prototype

chapter 4

ISSCC, JSSC 2021

Multi-threaded CPU execution

chapter 3

TDPS 2022